The Ultra 2 Workstation Architecture

Technical White Paper

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Ultra™— The Next Generation of Computing from Sun™

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The Ultra™ 2 workstation is an SBus-based, desktop multiprocessor system from Sun Microsystems. Offering exceptional performance in networking, graphics, I/O, and compute throughput, the Ultra 2 design underscores Sun's commitment to producing powerful and affordable multiprocessor UNIX® desktop systems.

Desktop Computing Performance

We have all seen examples of what is surely to be the future of computing — high speed networking that brings very large databases and advanced applications to distributed desktops; video conferencing that allows individuals in remote locations to interact as if they were in the same room; systems capable of running both advanced technical computing applications and popular personal productivity software; and object-oriented environments that shrink both development time and engineering costs. The intriguing demonstrations of these technologies aside, many computing platforms are simply not ready to deliver what is needed to make them a practical reality. Despite the raw power of many new processor families, the needed system performance is often just not there.

Experienced computing professionals understand that processor performance is a necessary component of any system intended for such use, but it is not sufficient. Advanced computing platforms must provide a balanced level of performance in many areas — memory access, I/O, graphics, networking, multiprocessing and multithreading, and CPU throughput — in order to avoid the bottlenecks that prevent them from achieving their full potential.

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A Continued Commitment to Computing Excellence

Over seven years ago, Sun™ engineers began to define a new computing architecture that would permit advanced applications to become a practical reality and not just a laboratory curiosity. Together, they developed a vision of computing practices and technologies that would define the standard for industry over the next decade. With this commitment, they began to outline the requirements that would have to be met in order to complete their vision:

- *Desktop Supercomputing*

  Sun engineers knew that the first measure of any desktop system is compute throughput. To meet the needs of their vision, they believed that performance nearing that of supercomputers would be required. Especially important for many applications would be very high floating point performance.

- *Visual Computing*

  The ability of high performance graphics to communicate complex ideas is well established. New was the need for such capabilities in less specialized technical and commercial environments. Sun's team reasoned that their next generation platforms would require committed processor resources to support strong graphics integration, 24-bit color, real time video, 3D graphics, and imaging.

- *Network Computing*

  To support the future needs of workgroup interaction, Internet access, and advanced enterprise computing, Sun engineers knew that 10 Mbps networking performance would be wholly inadequate. Future systems would require 100 Mbps Ethernet as well as efficient operation with even faster technologies like ATM and gigabit Ethernet.

- *Scalability and Binary Compatibility*

  Long ago, Sun appreciated the importance of scalable, binary compatible systems. In order to remain flexible, systems architectures must be part of a powerful family of compatible products, with each member capable of accepting upgrades to enhance performance and throughput. Any new platforms would need to be readily upgradeable and would have to remain binary compatible with the thousands of applications already available for Sun systems.

- *Software Interoperability and Productivity*

  Even in highly technical environments, corporate standards and individual requirements dictate that users must have access to popular personal productivity applications, such as those that run under Microsoft Windows. In addition, object computing and the Java™ programming language are reducing the cost and time to develop and deploy new applications. Sun's new definition demands that both of these needs be met with no compromises.

- *Workstation Quality and Technology*

  Workstations from Sun have long been associated with high levels of quality and reliability. Customers also know that with Sun, they can count on having access to the latest developments in systems and manufacturing technology. Future customers would demand no less.

- *Economy*

  One of principal attributes of Sun's vision is that it defines a standard for all desktop systems. The technologies just mentioned—CPU performance, advanced graphics, high speed networking, advanced software technology—would need to be accessible and affordable by everyone.

Sun Ultra™ Desktop Systems

Able to tackle the complex needs of networked-based multimedia, object-oriented environments, and visual computing, the Ultra 2 workstation is an SBus-based multiprocessing desktop platform designed to support the needs of business, science, education, and government (figure 1-1). Employing UltraSPARC-II processor technology, Ultra 2 delivers the performance needed by today's advanced applications:

- Software Development
- Electronic Design Automation (EDA)
- Financial Modeling
- Medical Imaging
- Earth Resources / GIS
- Visualization
- Molecular Modeling
- Collaborative Multimedia and Interactive Services
- 3-D Modeling and Simulation

First in the Ultra 2 lineup, the Ultra 2 Model 1300 workstation is configured with one 300 MHz UltraSPARC-II processor with 2 MB of external cache. Binary compatible with existing software, UltraSPARC-II processors accelerate existing applications and provides significantly higher levels of performance for those programs that have been prepared to exploit its design.

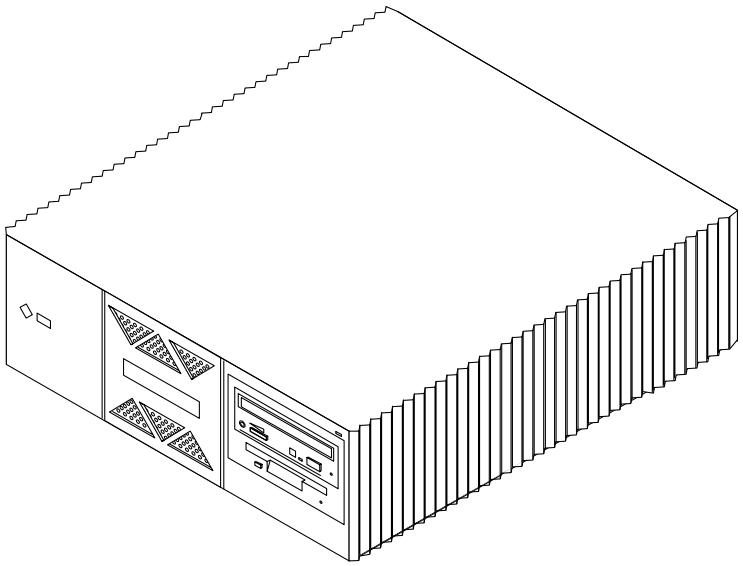

Figure 1-1 The Ultra 2 workstation is an SBus-based multiprocessing desktop platform designed to support the needs of business, science, education, and government.

The Ultra 2 Model 2300 offers great value to users needing to balance economy and performance in an SBus-based workstation. Equipped with dual 300 MHz UltraSPARC processors, users will enjoy outstanding integer, floating point, and multiprocessing throughput (12.3 SPECint95 and 20.2 SPECfp95). To complement their high performance processors, both the Model 1300 and 2300 includes standard Creator3D Graphics technology to dramatically accelerates video, 2-D and 3-D graphics, and imaging operations. For greater graphics throughput, users can elect to configure their Ultra 2 systems with Sun's highest performance framebuffer, the Elite3D.

Requirements for higher throughput can be easily met with the Ultra 2 Models 1400 and 2400. Employing one (Model 1400) or two (Model 2400) 400 MHz UltraSPARC-II processors, raw compute performance is significantly increased (17.2 SPECint95 and 25.9 SPECfp95 for the Model 2400). Like the Models 1300 and 2300, the Ultra 2 Models 1400 and 2400 can be equipped with standard Creator3D graphics, or Elite3D m6 framebuffers.

All Ultra 2 systems employ UPA, a low-latency, high performance, scalable interconnect between the processor, system memory, I/O, and graphics subsystems. To ensure balanced performance, autosensing 10/100 Mbps Fast Ethernet and Fast and Wide 20 MB SCSI is also standard. Memory capacity of Ultra 2 systems can reach as high as 2 GB using existing SIMM technology. Ultra 2 also features a standard complement of four SBus-compatible slots, serial and parallel ports, as well as 16-bit audio capabilities, 19 gigabytes of internal disk capacity, EPA Energy Star compliance, and a new, space-efficient desktop enclosure using 100% recycled plastic materials.

Like all new UltraSPARC-based systems from Sun Microsystems, Ultra 2 runs the Solaris Operating Environment™, Sun's benchmark implementation of System V Release 4 (SVR4) of the UNIX operating system, ensuring full binary compatibility with other Sun systems.

The Benefits of Multiprocessing

Multiprocessing like that found in the Ultra 2 increases productivity by running tasks in parallel — speeding database queries, providing remote file service, and accelerating computationally intensive applications. Sun's symmetric multiprocessing environment provides:

- flexibility to simply add or upgrade processors as needed
- binary compatibility across systems
- tools and related technologies to enhance the effectiveness of multiprocessing systems

Multiprocessing allows workstation users to reap tangible benefits by increasing performance in several ways. Often, these improvements can be realized immediately, without rewriting a single line of code:

- The multithreaded kernel of the Solaris Operating Environment enhances the inherent multitasking capability of UNIX. Multiple tasks can be spawned to run simultaneously on multiple processors. I/O functions, backups, windows management, and database searches can all run in parallel, improving the overall system performance and throughput.
- In most UNIX environments, users run more than one application simultaneously. Multiprocessing enhances performance and throughput because each application can run on a separate processor.
- Solaris can split application system calls into separate processes, each running in parallel. Graphics, networking, compute, and I/O requests can be run on different processors at the same time.
- Workshop developer toolkits include compilers to automatically detect parallelism and spread the execution of programs over many processors at run time.
- Multithreaded applications enhance productivity by decreasing the time it takes to perform one job. Developers can assign multiple tasks in a single application to independent threads of execution, with Solaris automatically assigning each thread to an available processor.

Ultra 2 Workstation System Overview 2

The Ultra 2 workstation line uses advanced materials, electronics, software, and fabrication technologies in their packaging, board design, subsystems, and components. This chapter briefly describes the Ultra 2 family. More detailed discussions of the processor, bus, graphics, and I/O architectures can be found in subsequent chapters.

Features Summary

- *Processors*

  One or two SPARC Version 9-compliant, 64-bit UltraSPARC-II processor modules, each with 2 MB of external cache, operating at 300 or 400 MHz.

- *ECC Protected Memory*

  128 MB to 2 GB using 5V DRAM SIMMs with 60 ns access time.

- *Standard Interfaces*

  100 Mbps IEEE 802.3 Fast Ethernet using twisted pair category 5 interfaces, downward compatible with 10 Mbps Ethernet (autosense). A Media Independent Interface (MII) is provided to allow use with ThickNet, twisted pair, ThinNet, or Fiber interfaces.

Fast and Wide, 20 MB/sec. single-ended SCSI-2, downward compatible with Fast 10 MB/sec. and standard 5 MB/sec. SCSI peripherals. Up to 15 SCSI devices are allowed (the six meter cable length restriction may impose a smaller number of devices in some configurations).

Four 64-bit wide IEEE 1496 (SBus) expansion slots and one UPA interface for a Creator3D or Elite3D m6 frame buffer.

Two RS-232/RS-423 serial ports and a Centronics-compatible parallel port.

16-bit, 48 KHz audio with line-out, line-in, microphone-in, headphone-out, and internal wide-range speaker.

Time of Day NVRAM for clock and ID functions.

Flash PROM for boot-time configuration. Can be reprogrammed in the field from a CD-ROM or over a local-area network.

- *Mass Storage*

  Supports one or two 1" 7200 RPM drives using Single Connector drive brackets.

  A 5.25” peripheral expansion bay, with room for an optional internal 5.25” 32x SCSI CD-ROM, 14 GB 8-mm tape drive, or 12-24 GB 4-mm DDS3 tape drive.

  3.5” 1.4 MB floppy supports three popular formats.

  Supports external QIC, 8-mm, and 4-mm tape, 4-mm tape stacker units, external disk arrays and disk storage units, and tape library systems.

- *Graphics*

  Standard third-generation high performance Creator3D Graphics technology includes improved performance over earlier implementations to match bus and processor speed improvements in the Ultra 2. Creator includes support for multiple monitor configurations and on-board color space conversion, 24-bit color, 1920 x 1200 and 1280 x 900 resolution, MPEG playback acceleration at 30+ frames per second, and image acceleration functions. Typical performance numbers for the Creator3D — 4.1 million X11 2D vectors per second, 3.7 million 3D vectors per second, 1.2 million triangles per second.

Those requiring the very highest graphics performance can choose the Elite3D m6 frame buffer. Elite3D m6 provides leading edge performance while retaining full upward compatibility with software written for Creator systems. It dramatically accelerates high-end functionality such as double buffering, triangle and quad rendering, and lighting and shading. In addition to high performance, Elite3D m6 incorporates on-board support for a wide array of important graphics functions. With six floating point units in the Elite3D m6, the results of performance tests are impressive: in excess of 4.7 million 2D vectors per second, 8.2 million 3D vectors per second, and 5.9 million triangles per second.

- *Input Devices*

  Sun Type 6. Opto-mechanical 3-button mouse is standard.

- *Software*

  Solaris 7. Solaris 2.5.1 (11/97), and Solaris 2.6 (3/98) are also supported. OpenWindows™ and Motif windowing systems. CDE desktop environment. ONC+™, NIS+, NFS™, TCP/IP networking technologies ensure maximum interoperability. Display Postscript™, XGL™, XIL™, OpenGL®, and Xlib graphics protocols to support a wide range of applications.

- *Reliability, Availability, and Serviceability (RAS) Features*
  - Extensive Power-on Self Test
  - ECC on all data transfers
  - Software memory scrubbing
  - Parity on cache RAMs
  - Temperature sensitive variable-speed fans
  - Internal thermal sensors control cooling
  - Thermal faults result in customer alerts and/or shutdowns to avoid component damage
  - SunVTS™ diagnostics can run at scheduled times to periodically validate system functionality
  - Simple clamshell enclosure for easy access to system components
  - Easily replaceable disks, SIMMs and graphics cards
  - Minimal internal cabling, with no cables for internal disks
  - Common fastener used throughout
  - Minimal use of jumpers
  - No I/O slot dependencies

- *Power Management*

  Ultra 2 platforms are Energy Star compliant, with the ability to automatically shut down after a predefined period of time. The pause-and-resume capability of Solaris allows users to quickly resume work in progress before the shutdown. Power management software also monitors the frequency of shutdown requests, and determines if the thermal shock of repeated power cycles would contribute to decreasing hardware reliability. If so, the shutdown request is deferred.

- *Specifications*

  Meets all relevant and domestic agency safety, ergonomics, EMI, and environmental requirements.

The UltraSPARC-II Processor

Implementing the SPARC version 9 architecture, the UltraSPARC-II processor retains complete backwards compatibility with the 32-bit SPARC V8 specification, ensuring binary compatibility with existing applications. Capable of 64-bit data and addressing, all UltraSPARC processors have a number of features to improve operating system and application performance:

- Better cache management and greatly reduced memory latency
- Built-in, low cost multiprocessor support
- Graphics and imaging support on chip
- Nine stage pipeline that can issue up to four instructions per cycle
- High performance both in SPECint95 (17.2) and SPECfp95 (25.9) at 400 MHz
- High efficiency trap management

In addition to support for standard UltraSPARC features, UltraSPARC-II incorporate several improvements over UltraSPARC-I:

- Implemented using 0.35 micron, 5-layer metal CMOS technology operating at 3.3 and 2.6 volts. Packaged using a 787-pin Land Gate Array (LGA)
- On-chip 16 KB Data and 16 KB Instruction cache, with up to 16 MB external cache allowed (2 MB maximum in Ultra 2 systems)
- Support for data prefetch and multiple outstanding memory requests
- Improved UPA interconnect architecture clocked at 100 Mhz permits high speed memory transfers of 1.6 GB/sec.

UPA Interconnect

Key to the performance of the Ultra 2 workstation is Sun's exclusive Ultra Port Architecture technology. Implemented as a cache-coherent interconnect between processor, memory, graphics, and I/O subsystems, UPA offers several advantages over existing interconnects:

- Increased performance over previous 83 Mhz designs
- Packet switched for better bus utilization
- Low latency memory accesses
- Precise interrupt processing
- Buffered cross bar memory interface for increased bandwidth and greatly improved scalability
- High throughput paths to memory clocked at 100 Mhz (576-bit wide paths on Ultra 2, including ECC)
- More economical implementation through centralized coherence and memory controller functions
- Integrated support for multiprocessor configurations

Graphics

Sun has long appreciated the importance of high performance graphics in the technical workstation market, and today, they offer products with some of the best graphics price-performance available anywhere. This trend continues with the availability of high performance framebuffers like the third-generation Creator3D Graphics capabilities standard on Ultra 2 systems. Creator Graphics improvements include higher levels of performance than earlier models, support for high resolution monitors, and enhancements for video decompression:

- Features include standard 24-bit color, 1280 x 1024 resolution (1920 x 1200 with Creator3D in single buffer mode), MPEG playback acceleration at 30+ frames per second, >5.1 million 2D vectors per second, >3.7 million 3D vectors per second, over 1.4 million triangles per second, and on-board image acceleration functions.
- YCC to RGB color space conversions for faster video decompression
- Numerous design improvements, including higher internal clocking, allows Creator Graphics performance to exceed that of previous generations.

Ultra 2 also supports the Elite3D m6 graphics accelerator. Featuring a design completely upwards compatible with Creator3D, Elite3D m6 adds significantly higher levels of performance and functionality:

- Standard 24-bit color, 1280 x 1024 resolution, MPEG playback acceleration at 30+ frames per second, >5 million 2D vectors per second, >8.2 million 3D vectors per second, 5.9 million triangles per second, and on-board image acceleration functions.
- Elite3D m6 include 88 bit planes, including full 24-bit double-buffer planes for smooth animation. A 28-bit Z-buffer is included to provide support for hidden surface removal and dynamic rendering of 3D objects.
- Support for a wide array of important graphics functions, including Bresenham lines; polygons; fonts; accelerated dots, lines, triangles, and quadrilaterals; antialiasing of dots and lines; Gouraud shaded triangles; specular lighting; hardware per-pixel depth cueing; transparency; texture map support; compressed 3D geometry decompression; viewport clipping; flexible blending operations; and a full set of Boolean operations.

Other features common to both Creator3D and Elite3D m6 include:

- Sun / Mitsubishi developed 3D-RAM to improve 3D graphics rendering performance
- Exploits the high floating point performance and VIS Instruction Set of the UltraSPARC-II processor
- High speed RAMDAC can display 8-bit and 24-bit images simultaneously, and features a programmable video timing generator for multiple resolution support
- Completely compatible with existing Sun graphics APIs, including X11, XGL, XIL, and OpenGL.

Networking and I/O

All Ultra 2 models provide on-board 100 Mbps Fast Ethernet which can autosense and drop to 10 Mbps operation. Also standard is Fast and Wide SCSI accessible through a standard 68-pin connector. Completely compatible with earlier Fast (10 MB / sec.) and standard (5 MB / sec.) SCSI peripherals, all Ultra 2 systems can accommodate up to 15 SCSI devices subject to cable length limitations.

In addition, Ultra 2 models provide comprehensive expansion options:

- Supports one or two 1" drives using Single Connector drive brackets
- Internal bay includes room for a 5.25” peripheral, including an optional internal SCSI CD-ROM, 12-24 GB DDS3 4-mm tape, or 14 GB 8-mm tape drives
- 3.5” 1.4 MB floppy supports three popular diskette formats
- Supports external disk expansion, QIC, 8-mm, and 4-mm tape, and 4-mm tape stacker units
- Support for external disk array (RAID) and tape library systems for high reliability storage and backup needs
- The Ultra 2 lineup includes support for 64-bit SBus connectivity, yet retains compatibility with existing SBus products. Four SBus slots are provided.
- Selected peripherals from earlier Sun desktops can be used on both UItra 2 models to preserve existing investments in hardware

The Ultra 2 backpanel includes a number of other standard input/output connectors for external connection to networks, SCSI, parallel and serial peripherals, and audio equipment. Ultra 2 systems use full-sized connectors throughout without requiring the use of special “splitter” cables.

Enclosure and Power

The desktop enclosure for Ultra 2 systems is designed to accommodate easy access, ample room for upgrades, optimized system board layout, and space for standard connectors on the back panel. Measuring 5.1” high by 17.7” wide by 17.3” deep, the Ultra 2 enclosure includes space for two 1" drive bays, four SBus modules, a UPA slave expansion module, 16 SIMM slots, a half-height 5.25" peripheral bay, and one half-height 3.25" bay for a floppy drive (figure 2-1).

The power supplies in Ultra 2 systems are designed with better power-dissipation characteristics and to support 3.3V operation for UltraSPARC. The Ultra 2 power supply also supports programmable core voltages. To ensure optimum cooling, Sun has made use of innovative, internal plastic plenums to regulate airflow within the enclosure.

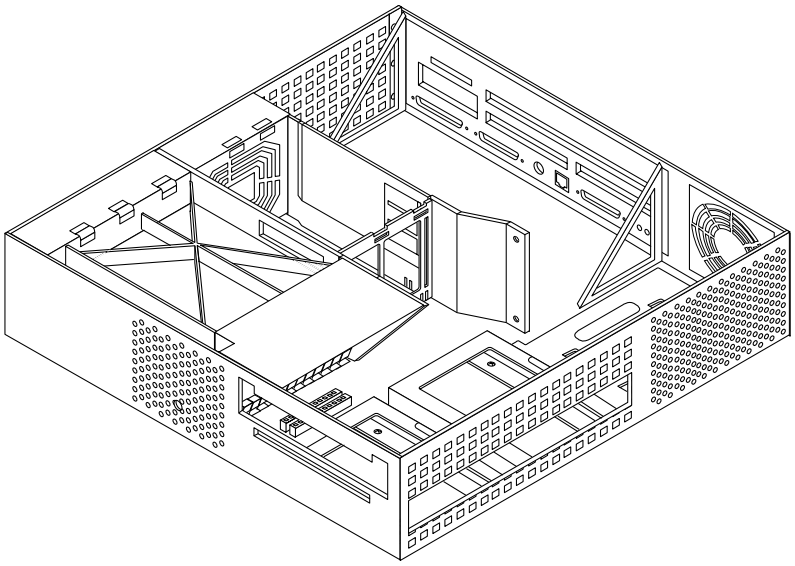

Figure 2-1 Ultra 2 accommodate peripheral expansion through two 1" drive bays, a half-height CD-ROM bay, and one half-height bay for a diskette drive.

Sun has also recognized the need for environmentally sensitive construction and operation with Ultra 2. The enclosures are made from 100% recycled plastic materials, and are themselves recyclable. Ultra 2 is also EPA Energy Star compliant, featuring an automatic shutdown after a programmed period of time. With Ultra's pause-and-resume capability, users can quickly restore all work in progress before the shutdown.

The Ultra 2 Architecture 3

The Ultra 2 architecture was designed to provide high performance, scalability, reliability, and flexibility without compromising economy. The very high levels of integration achieved with Ultra 2 systems through the use of application specific integrated circuits (ASICs) have resulted in a greatly reduced part count, high reliability, and low cost without compromising access to a full complement of expansion options through high performance, standardized interfaces.

The following pages describe the Ultra 2 architecture in detail, beginning with a system block diagram (figure 3-1). Because many of the subsystems of Ultra 2 systems are integrated directly into the UltraSPARC-II microprocessor, considerable attention is given to it. In addition, the memory subsystem, interconnect architecture, significant ASICs, and available peripherals are described. Because the Ultra 2 has some very special graphics capabilities, a separate chapter describing them immediately follows this one.

The UltraSPARC-II Microprocessor

The SPARC Version 9 Architecture

SPARC has been implemented in processors used in a range of computers from laptops to supercomputers. SPARC International member companies have implemented over twenty different compatible microprocessors since SPARC was first announced—more than any other RISC (reduced instruction set computing) microprocessor family. As a result, SPARC today boasts the

support of over 12,000 compatible software and hardware products. SPARC Version 9 maintains upwards binary compatibility for application software developed for previous SPARC implementations, including microSPARC™, TurboSPARC™, and SuperSPARC.

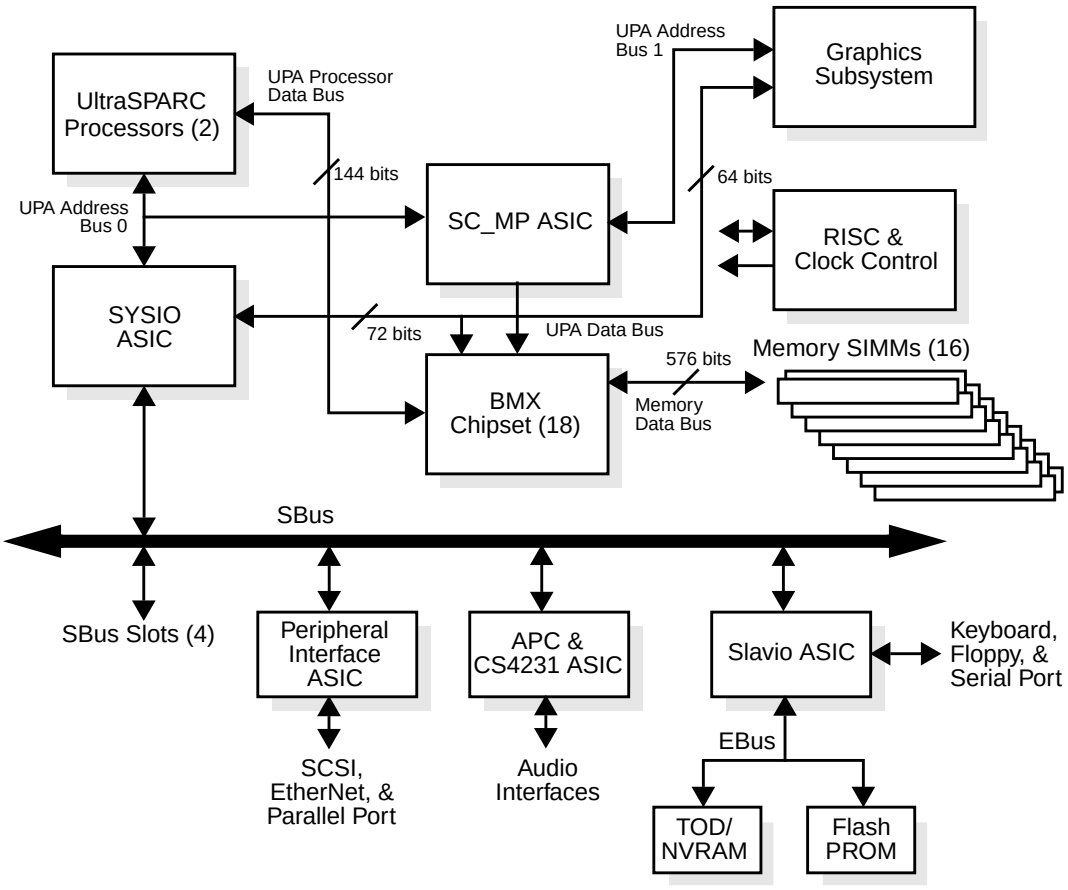

Figure 3-1 Architecture of the Ultra 2 workstation.

SPARC-V9 represents a significant advance for the microprocessor industry. It provides 64-bit data and addressing, fault tolerance features, fast context switching, support for advanced compiler optimizations, efficient design for

superscalar processors, and a clean structure for emerging operating systems. And all of this has been accomplished with 100-percent binary compatibility for existing SPARC-based application programs.

UltraSPARC-II

UltraSPARC–II is a high-performance, highly-integrated superscalar processor implementing the SPARC-V9 64-bit RISC architecture. The UltraSPARC–II is capable of sustaining the execution of up to four instructions per cycle even in the presence of conditional branches and cache misses. This sustained performance is supported by a decoupled Prefetch and Dispatch Unit with Instruction Buffer. Load buffers on the input side of the Execution Unit, together with store buffers on the output side, completely decouple pipeline execution from data cache misses. Instructions predicted to be executed are issued in program order to multiple functional units and execute in parallel. Such predictively-issued instructions can complete out of order. In order to further increase the number of instructions executed per cycle, instructions from different blocks (for instance, instructions before and after a conditional branch) can be issued in the same group.

UltraSPARC-II is part of a second generation of UltraSPARC pipeline-based products. In addition to using a new process technology, the UltraSPARC-II provides a higher clock frequency, multiple SRAM modes and system-to-processor clock ratios to accommodate varying economics for a range of products. At the same time, it provides software compatibility with existing UltraSPARC-I based systems. UltraSPARC-II also implements the SPARC-V9 PREFETCH instruction.

The UltraSPARC–II supports both 2D and 3D graphics as well as image processing, video compression and decompression, and video effects through the sophisticated VIS Instruction Set. VIS provides high levels of multimedia performance, including real-time H.261 video compression / decompression and two streams of MPEG-2 decompression at full broadcast quality with no additional hardware support.

Key Features of the UltraSPARC-II

The newest member of Sun's family of SPARC CPUs, UltraSPARC-II is the most sophisticated of the SPARC family of processors to date. Designed for use in uniprocessor and multiprocessor systems, UltraSPARC-II offers the following key features:

- SPARC Version 9 architecture compliant
- Binary compatible with all existing SPARC applications
- VIS Instruction Set to support advanced multimedia capabilities
- Multiprocessing support includes glueless four-processor connections with minimum latency
- Snooping or directory-based bus protocol support
- Four-way superscalar design incorporating nine execution units—four integer execution units (IEUs), three floating-point execution units (FPUs), and two graphics execution units (GRUs)
- Software PREFETCH instruction support and multiple outstanding requests support
- Selectable little- or big-endian byte ordering
- 64-bit address pointers that enjoy transparent compatibility with 32-bit addressing
- 16 KB non-blocking data cache
- 16 KB Instruction Cache featuring in-cache 2-bit branch prediction and single cycle branch following
- Integrated second-level cache controller supports 0.5 to 16 MB caches. Sustained throughput of 1 load per cycle and 2.6 GB/sec. processor-cache bandwidth
- Block Load/Store Instructions combined with 1.9 GB/sec. processor-memory bandwidth results in sustained processor-memory transfers of nearly 400 MB/sec.
- Includes JTAG boundary scan and special performance instrumentation to support product development and testing
- Employs 0.35 micron five-layer metal CMOS process. Operates at 3.3V and 2.6V.
- Use of 787-pin Land Grid Array.
- On-chip power management

UltraSPARC-II Functional Units

In a single chip implementation, the UltraSPARC-II processor features a very high level of integration which include the following components (figure 3-2):

- A prefetch, branch prediction, and dispatch unit
- 16 KB instruction and data caches
- An MMU composed of a 64-entry instruction translation lookaside buffer (TLB) and a 64-entry data TLB
- An integer execution unit with two ALUs
- One load/store unit with a separate address generation adder
- A load and store buffer which decouples data accesses from the pipeline
- A floating-point unit with independent add, multiply, and divide/square root sub-units
- A graphics unit with two independent execution pipelines
- An external cache controller
- A unit responsible for main memory and I/O accesses

Prefetch and Dispatch Unit

The prefetch and dispatch unit fetches instructions before they are actually needed in the pipeline so that the execution units do not starve for instructions. Instructions can be prefetched from all levels of the memory hierarchy, including the instruction cache, the external cache, and main memory. To prefetch across conditional branches, a dynamic branch prediction scheme is implemented in hardware. The outcome of a branch is based on a two-bit history of the branch. A *next field* associated with every four instructions in the instruction cache (I-cache) points to the next I-cache line to be fetched. The use of the next field makes it possible to follow taken branches and provide the same instruction rate as running sequential code. Prefetched instructions are stored in the instruction buffer until they are sent to the rest of the pipeline. Up to 12 instructions can be buffered.

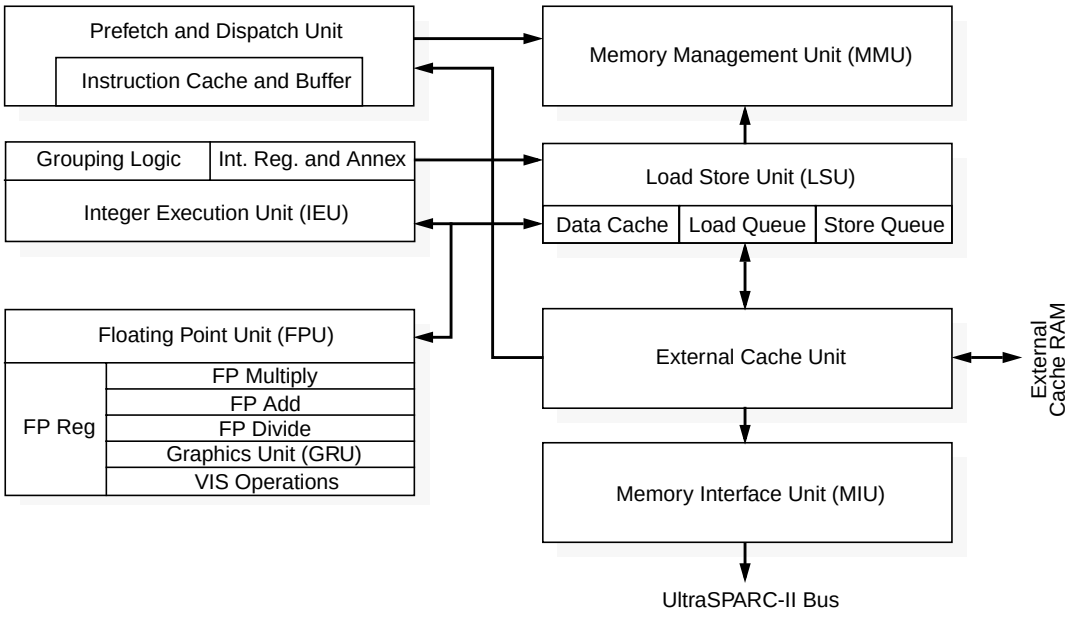

Figure 3-2 UltraSPARC-II functional block diagram.

Instruction Cache

The instruction cache is a (pseudo) 16 KB two-way set associative cache with 32-byte blocks. The cache is physically indexed and contains physical tags. The set is predicted as part of the next field so that only the index bits of an address are necessary to address the cache (13 bits which matches the minimum page size). The instruction cache returns up to 4 instructions from an 8 instruction-wide line.

Data Cache

The data cache (D-cache) is a write-through, non-allocating 16 KB direct mapped cache with two 16-byte subblocks per line. It is virtually indexed and physically tagged. The tag array is dual ported to ensure that tag updates due to line fills don’t collide with tag reads for incoming loads. Snoops to the D-cache use the second tag port to allow incoming loads to proceed without being held up by a snoop.

Memory Management Unit (MMU)

The MMU provides mapping between a 44-bit virtual address and a 41-bit physical address. This is accomplished through a 64-entry translation lookaside buffer (TLB) for instructions and a 64-entry TLB for data, both fully associative. UltraSPARC-II provides hardware support for a software-based TLB miss strategy. A separate set of global registers is available whenever an MMU trap is encountered. Page sizes of 8K, 64K, 512K, and 4 Mbytes are supported.

Integer Execution Unit (IEU)

Two ALUs form the main computational part of the IEU. An early-out multi-cycle integer multiplier and a multi-cycle integer divider are also part of the IEU. Eight register windows and four sets of global registers are provided (normal, alternate, MMU, and interrupt globals). The trap registers (UltraSPARC-II supports five levels of traps) are also part of the IEU.

Load/Store Unit (LSU)

The LSU is responsible for generating the virtual address of all loads and stores, for accessing the data cache, for decoupling load misses from the pipe through the load buffer, and for decoupling the stores through a store buffer. One load or one store can be issued per cycle. To further optimize data stores, a store compression capability allows two or more stores to be “compressed” together if they are in the same 16-byte block, so that a single data transfer occurs between UltraSPARC and the second-level cache. This frees up the data bus allowing load misses and instruction misses to be processed more rapidly.

Floating-Point Unit (FPU)

The separation of the execution units in the FPU allows UltraSPARC-II to issue and execute two floating-point instructions per clock cycle. Source data and results are stored in a 32-entry register file, where each entry can contain a 32-bit value or a 64-bit value. Most instructions are fully pipelined, (throughput of one per cycle) have a latency of three cycles, and are not affected by the precision of the operands (single or double precision operations have the same latency). The divide and square root instructions are not pipelined. They require 12 cycles (single precision) or 22 cycles (double precision) to execute but do not stall the processor. Other instructions following the divide or square root instructions can be issued, executed, and retired to the register file before

the divide or square root instructions finish. A precise exception model is maintained by synchronizing the floating-point pipe with the integer pipe and by predicting traps for long latency operations.

Graphics Unit (GRU)

UltraSPARC-II provides a comprehensive set of graphics instructions that provide fast hardware support for 2D and 3D graphics, image manipulation and compression, and video and audio processing. 16-bit and 32-bit partitioned add, boolean, and compare are provided as are 8-bit and 16-bit partitioned multiplies. Single-cycle pixel distance, data alignment, packing, and merge operations are all supported in the GRU.

External Cache Unit (ECU)

It is the responsibility of the ECU to efficiently handle I-cache and D-cache misses. The ECU can handle one access per cycle to the external cache. These low latencies can effectively make the external cache a part of the pipeline. For programs with large data sets, this means data can be maintained in the external cache and instructions scheduled with load latencies based on the E-Cache latency. Floating-point applications can use this feature to effectively “hide” D-Cache misses. The size of the external cache can be 512 Kilobytes, 1-, 2-, 4-, 8-, or 16 Megabytes, where the line size is always 64 bytes. A MOESI protocol is used to maintain coherency across the system.

The ECU provides overlap processing during load and store misses. For instance, stores that hit the E-Cache can proceed while a load miss is being processed. The ECU is also capable of processing reads and writes indiscriminately without a costly turnaround penalty (only 2 cycles are needed). Snoops are also handled by the ECU.

Block loads and block stores load or store a 64-byte line of data from memory to the floating-point register file. These are processed efficiently by the ECU, providing high-transfer bandwidth without polluting the internal or external cache.

Memory Interface Unit (MIU)

All transactions to the system, such as external cache misses, interrupts, snoops, and writebacks, are handled by the MIU. The MIU communicates with the system at a frequency lower than UltraSPARC–II frequency (the ratio can be 1/2, 1/3, 1/4, or 1/5). Both the MIU and the ECU provide support for multiple outstanding load and writeback requests to the Ultra Port Architecture (UPA) bus.

VIS™ Instruction Set

UltraSPARC is the first microprocessor to fully support advanced multimedia and networking. By introducing a comprehensive set of multimedia instructions, known as the VIS Instruction Set, UltraSPARC provides enhanced hardware support for 2D and 3D graphics, video and audio processing, and image manipulation.

The graphics unit in UltraSPARC-II relies on the integer registers for addressing image data and the floating point registers for manipulating image data. This division of duty between the integer and floating point registers enables UltraSPARC-II to make use of all available internal registers, maximizing throughput.

Pixel information in UltraSPARC-II consists of four 8-bit integer values. These four values represent the color (RGB) and intensity information for a color image. For higher resolution images, like those used in medical or color imaging, UltraSPARC-II also supports 16-bit pixels. Support is provided both for band-interleaved images, with the various color components stored together, and band-sequential images that have all of the values for one color component stored together.

Intermediate results for advanced image manipulation are stored as 16- or 32-bit, fixed-data values. These provide an intermediate format with enough precision and dynamic range for filtering and image computations on pixel values. UltraSPARC-II has several single-cycle instructions specifically tailored for manipulating these 16- and 32-bit components.

UltraSPARC-II also includes a variety of instructions that are essential for advanced image manipulation. For example, UltraSPARC-II supports a filtering operation for scaling, rotating, and smoothing images. The filtering operation processes four pixels at a time, giving UltraSPARC-II an order of magnitude performance advantage over other processors.

Able to perform motion estimation in support of motion compensation, a technique used to code real-time video for compression, the UltraSPARC-II can greatly accelerate multimedia applications. Motion estimation takes advantage of the minimal changes in the position of images from one frame to the next. The processor performs hundreds of comparisons for a region of the image, searching for a motion value that minimizes the estimation error. The error is calculated by summing the differences for each pixel in the region between a reference frame and a newer frame.

UltraSPARC-II minimizes this compute-intensive operation by operating on eight pixels at a time. The motion compensation process for eight pixels requires eight subtractions, eight absolute values, eight additions, a load of eight pixels, an align of eight pixels, and one final addition. UltraSPARC-II performs this complex set of operations for eight pixels in just one clock compared to the minimum of 48 instructions and numerous clocks typically required by other processors. Because motion estimation is the dominant operation for compression, UltraSPARC-II's high throughput for this operation allows it to support compression for desk-top video conferencing without the aid of external circuitry.

Unique block load / store commands in UltraSPARC-II allow the processor to execute 64-byte loads and stores directly into main memory. The block load / store commands avoid “cache pollution” by eliminating data allocation to external cache. With the resulting high copy bandwidth, UltraSPARC-II can move images directly from main memory to the screen fast enough to eliminate image flicker.

Although VIS was created to accelerate the manipulation of graphics data, it handles other types of partitioned data just as well. Other uses of VIS include the processing of audio data and in encryption / decryption applications.

Additional papers and documents devoted to VIS and VIS programming are available from Sun. See the References appendix for more details.

Cache Architecture

Virtually all high-performance microprocessors use cache to reduce bus traffic and increase system throughput. Cache stores contain copies of part of a memory image. The choice of whether to update or invalidate copies of modified blocks is part of the *cache coherency protocol*. These protocols ensure

that copies of data remain consistent. UltraSPARC-II supports several protocols, including write-invalidate, write-broadcast, and competitive caching algorithms.

External cache accesses are independent with respect to other instructions (e.g. ALU operations) and are not closely coupled to the pipeline. Full throughput to the external cache is supported and can make it look like a very large D-cache. The micro architecture used to support this consists of the load buffer, separate address busses for tag and data, etc.

The external cache consists of Tag RAM, which contains the physical tags of the cached lines and three bits of state information, and the external cache Data RAM, which contains the actual data for each cache line. Both operate synchronously with UltraSPARC-II. The UltraSPARC-II can support cache sizes as large as 16 Mbytes (although the accompanying processor subsystem must be design to accommodate this cache maximum). The actual cache size is determined at boot time by software. Each byte in the RAMs is accompanied by a parity bit (three bits for the tags and 16 bits for data).

Fast Traps and Context Switching

Fast traps and context switching have also been provided in UltraSPARC-II, with the trap entry mechanism re-architected to transfer control into the trap handlers very quickly. Eight new registers, called “alternate globals”, provide the trap handler with a fresh register to use immediately upon entry. Moreover, the trap handler software need not store registers before it starts to execute, permitting very fast instruction emulation and extremely short interrupt response times.

The number of registers saved and restored between process executions has also been reduced, resulting in faster context switches. The architecture provides separate dirty bits for the original (lower) and the new (upper) floating-point registers. If a program has not modified any register in one of the sets, unnecessary register saves during a context switch can be avoided.

3

Memory Subsystem

External Cache Memory

Ultra 2 models feature 2 MB of external secondary cache with 64-byte line size. Synchronous SRAMs are used for data and for tag. The datapath to the external cache is 128-bits wide and is parity protected with 16 bits of parity (1 bit per byte).

Main Memory

The Ultra 2 desktop systems have a memory system which uses conventional 5V DRAM SIMMs with a 60 nanosecond access time. They are identical to the SIMMs used in other Ultra workstations and in previous generation SPARCstation™ 20 systems, allowing the retirement or replacement of systems without sacrificing large investments in memory.

The systems allow for the use of 16 SIMM modules, with supported module sizes including 32 MB, 64 MB, and 128 MB. Maximum memory capacity is 2 GB using 128 MB modules.

SIMMs must be added to Ultra 2 systems in sets of four. It is recommended that each set be the same size, as the largest SIMM of the set will be treated as if its capacity were equivalent to the smallest SIMM.

Ultra 2 systems feature adjustable memory timing to ensure near-constant latencies and bandwidth across the range of bus frequencies.

The Ultra Port Architecture (UPA) Interconnect

Needing to ensure the correct balance between the high performance computational and graphic subsystems in Ultra, Sun set about creating the Ultra Port Architecture (UPA) by starting with some very demanding requirements, including reduced memory latency, lower cost, and optimized price/performance for uniprocessor and multiprocessor systems.

Engineers responded to these requirements with UPA, a cache-coherent processor-memory interconnect. As implemented in the Ultra 2, the principal advantages of the UPA over existing interconnects are significant:

- Scalable bandwidth through support of multiple bussed interconnects for data and addresses
- Higher bandwidth
- High performance graphics support with two-cycle single-word writes on the 64-bit UPA interconnect
- Better economy through centralized coherence and memory controller functions

UPA Interconnect Implementation

In the Ultra 2, the UPA interconnects employ several advanced technologies:

- The UPA clock can operate at up to 100 Mhz in the Ultra 2.
- Nine buffered crossbar circuits are used to connect the two 144-bit processor data paths to 576-bit memory bus and two 72-bit (64 bits of data) I/O and graphics buses.
- Overlapped transfers on multiple UPA segments are supported.
- A system controller ASIC integrates memory controller functionality, controls the crossbar circuits, and permits maximum memory configurations of 2 GB.

The UPA Interconnection Model

The UPA interconnection model comprises several components (figure 3-3). They include UPA ports, the system controller, memory, and datapaths.

UPA Ports

A UPA port is the interface to the interconnect. A UPA module logically plugs into a UPA port, and may contain a processor, an I/O controller with interfaces to I/O busses, or a graphics frame buffer. A UPA port has separate packet switched address and data busses which operate independently. The UPA interconnect architecture supports up to 32 UPA ports and multiple address and data busses. Up to four UPA ports can share the same address bus, and arbitrate for bus master status through a distributed arbitration protocol.

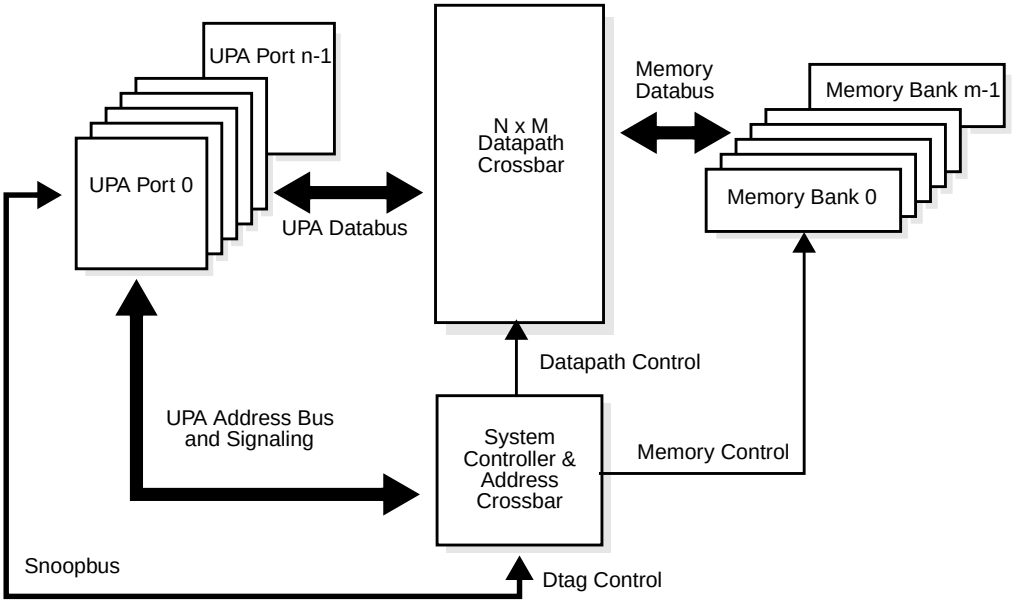

Figure 3-3 Typical UPA interconnect configuration

A UPA port has four functional interface properties which classify it as a *master*, *slave*, *interrupter*, or *interrupt handler*. A UPA port is identified by a 5-bit *port_ID* field. At a minimum, a UPA port must implement the slave interface and the port_ID register.

System Controller

The system controller is a centralized controller and provides coherence control, memory and datapath control, and crossbar-like connectivity for multiple address busses.

Datapaths

The datapath in the UPA interconnect model can be a N x M switch, or it can be a bus, or a combination of the two. The exact organization of the datapath is implementation specific. The system controller controls the datapath, and schedules the transfer of data between two UPA ports, or between the UPA port and memory.

The UPA address bus is a 36-bit, bidirectional packet-switched request bus, and includes 1-bit odd parity. In two cycles, it carries the high-order 37 bits of a 41-bit physical address space, the lower four bits being implied to provide 16-byte addressibility. UPA ports do not communicate directly on the UPA address bus. Instead, the system controller forwards a slave access to the addressed port by retransmitting the request packet after qualifying the destination port. A UPA port does not snoop on the UPA address bus. This too is done by the system controller on behalf of caching master UPA ports using a write-invalidate cache coherence protocol.

UPA data busses are either 128- or 64-bits wide with 16 or 8 additional bits for ECC. Although the 64-bit wide UPA data bus has half as many pins, it carries the same number of bytes per transaction as the 128-bit bus, but in twice the number of cycles. The interconnect does not generate or check ECC. This is the responsibility of the source and destination UPA ports. (Master UPA ports must support ECC, while slave ports need not do so.)

UPA data busses are not a globally shared common data bus. There may be multiple UPA data busses in the system, the precise number being implementation specific.

Memory

The architecture supports an arbitrary number of memory banks, the exact number being implementation specific (16 SIMM slots in the case of Ultra 2). The system controller controls the memory timing in conjunction with datapath scheduling to optimize the utilization of both.

The system controller, the datapath, and the memory are in the interconnect domain, and are abstracted from the UPA module by the UPA port interface. The interconnect domain is fully synchronous with a centrally distributed system clock which is also sourced to the UPA modules. If desired, the UPA module can synchronize its private clock with the system clock.

Features of the UPA Interconnect

Incorporating many features previously found only on mainframes and high performance servers, the UPA interconnect architecture incorporates several innovations designed to meet the ambitious requirements of Ultra platforms. Unlike conventional cache-coherent systems which use a globally shared snooping address bus, the UPA interconnect architecture relies on point-to-point packet switched messages from a centralized system controller to maintain cache coherence. Packet switching provides for much better bus bandwidth utilization by removing the latencies commonly associated with pure transaction-based designs.

Unlike other directory-based systems which maintain the coherence states for each data block in main memory, requiring a read-modify-write penalty for every read transaction that reaches main memory, the UPA interconnect maintains a duplicate set of all cache tags in the system and performs duplicate tag lookup and main memory initiation in parallel pipelines for each coherent transaction. This departure from conventional approaches permits minimum latency on cache misses, and effective pipelining in the interconnect allows maximum, and often “bubbleless” utilization of address, datapath, and main memory.

The design of the UPA interconnect was targeted to single processor and multiprocessor workstation systems. One result of this was the use of a centralized system controller, which removed the need to place cache coherence logic on each processor and DMA device, considerably simplifying the implementation.

Other key features of the UPA interconnect include:

- *Independent address and data*

  UPA was designed to accommodate desktop SMP systems. As a result, it can accommodate multiple address and data busses to avoid throughput bottlenecks. This approach also produces significant improvements in uniprocessor implementations by removing the need to share address and data lines.

- *Independent operation of I/O and processor busses*

  Overall system throughput is increased by decoupling the operation of the I/O and processor busses.

- *Use of precise interrupts*

  Like other transactions, interrupts in the UPA interconnect environment are also handled through the delivery of a packet from the interrupting device. The packet provides sufficient information for the processor and service routines to begin immediate processing of the interrupt, greatly reducing the interrupt service routine latency.

- *Streaming buffer*

  A technology previously available only on more expensive server systems, the use of streaming buffers allows devices capable of Direct Virtual Memory Access (DVMA) to achieve much higher levels of performance by reducing the bus busy times during data acquisition and delivery.

- *Major busses protected by parity or ECC*

  In an unusual move to ensure the highest reliability, Sun engineers have implemented parity protection on the UPA address bus, and ECC protection on the UPA data bus as well as between the crossbar and memory.

SBus Connectivity, Peripherals, and Back Panel

Ultra 2 desktop systems support four SBus slots accessible through the back of the enclosure. The SBus slots allow expansion to a variety of I/O options, including network interfaces such as ATM, ISDN and Fibre Channel, graphics adapters, printer interfaces, and hundreds of third-party SBus cards.

SBus specifications for the Ultra 2 systems include:

- 25 Mhz operation (independent of processor and UPA operating frequencies)
- Conformant to IEEE 1496 standards for SBus operation — compatible with all existing SBus peripherals
- Extended transfer mode (64-bit wide data bus)
- Transfer sizes up to 64 bytes
- Parity checking
- Dedicated interrupt per SBus slot

In addition to SBus connectivity, all Ultra models support a standard complement of I/O devices through connectors on the back panel (figure 3-4):

- Ethernet
- Audio port

- Serial-ports and Centronics-compatible parallel port
- SCSI
- Keyboard / Mouse

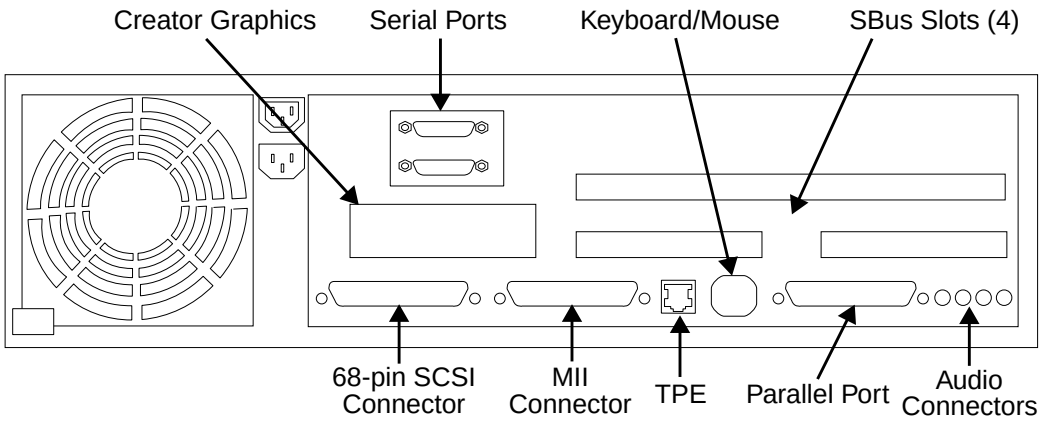

Figure 3-4 Ultra 2 Model 2200 backpanel connectors

Ethernet

To support higher performance network connectivity, all Ultra 2 models support 10 / 100 Mbps Fast Ethernet. Fast Ethernet technology from Sun is backwards compatible with 10 Mbps Ethernet, with the speed being autosensed by the interface.

Fast Ethernet is a direct extension of the 10Base-T Ethernet standard, but is capable of supporting a wider range of applications requirements with its greater throughput. Particularly compelling is its compatibility with the installed base of wiring currently employed for 10Base-T, making it the most cost-effective migration path for most users. Like its predecessor, the standards for Fast Ethernet are well defined and accepted throughout the industry, and a large number of compatible products are available from a variety of vendors.

The Ethernet interface on the Ultra 2 systems support access to Category 5 twisted pair through an RJ45 connector. To support a wider array of cabling options, they also feature access to a Media Independent Interface (MII).

Accessible through a 40-pin, miniature “D” connector, the MII allows adoption to any other form of Ethernet, including ThickNet (AUI), twisted pair, ThinNet, or Fiber.

Audio

The logic board and system enclosure allow Ultra systems include high-quality audio circuitry on the motherboard and an internally-mounted speaker.

All systems also support a variety of standard sampling rates, including:

- 16-bit 48-KHz Digital Audio Tape (DAT)
- 16-bit 44.1-KHz CD
- 16-bit, 16-KHz medium-quality audio for applications such as speech processing
- 8-bit 8-KHz standard telephony

The backpanel provides a variety of audio connectors allowing the Ultra 2 systems to be connected to standard audio equipment such as amplifiers and tape recorders. A small mono external microphone is provided, making audio input and output more convenient. Keyboard controls are included for volume control.

Parallel Port

The usefulness of parallel ports on desktop machines has grown due to the increased availability of peripherals that use them, especially low-cost, high-quality printers. And with data rates up to 2 MB/sec, the bidirectional parallel port can be used for other applications such as data acquisition, scanning, and high speed communications.

The parallel port can operated using programmed I/O or DMA. Its interface direction, timing, and protocol is programmable to meet the wide variety of Centronics interfaces that exist on peripheral devices.

Access to the parallel port is through a DB25 connector located on the backpanel.

Serial Ports

RS-232C and RS-423 serial ports provide a convenient way to connect an Ultra system to devices such as modems and terminals. Two serial ports are provided, each with independent DB25 connectors with standard pinouts. Synchronous transfers can occur at 64 Kbps, while asynchronous transfers can occur at up to 76.8 Kbps.

SCSI

All Ultra 2 systems include a Fast and Wide, 20 MB/sec. SCSI interface. A total of 15 internal and external SCSI peripherals can be connected to the same daisy chain, with external peripherals accessible through a 68-pin “D” type SCSI connector. (50-pin connectors can be used with the addition of an adaptor cable.) Maximum cable length is approximately 6 meters, including 0.9 meters for internal cabling.

Keyboards and Mice

Standard with each Ultra system is a Sun Type-6 keyboard which has a layout compatible with the common IBM AT 101-key keyboard.

Keyboard and mice connect in series to an 8-pin DIN connector located on the back panel. Ultra 2 come with a standard three-button opto-mechanical mouse.

Graphics 4

Sun understands that graphics is rapidly shifting away from being a specialized requirement of technical users and is becoming an essential part of nearly every computing discipline. Sun believes that as this trend continues, the standards for graphics functionality and performance will continue to rise. Ultra 2 systems anticipate this trend by providing standard graphics capabilities that rival the performance of products available only as options on other desktop systems.

When designing the first Ultra systems, Sun engineers set out to build a graphics architecture that could not only withstand the rigors of current requirements, but one that could excel and scale for years to come. It quickly became apparent that such a goal demanded a complete rethinking of basic requirements:

- *Best of the best performance*

  The new graphics platform should have at least twice the peak performance of the previous generation accelerators in the areas where they excelled.

- *Best of the best functionality*

  The functionality of previous generation frame buffers is supported, but with greater performance.

- *More standard functionality*

  Features like 24-bit graphics, video decompression, 3D graphics, and high resolution should be a standard part of the system, not expensive options.

- *Cost effective*

  The new graphics system needed to be economical enough to be included as standard equipment on high performance desktops. This implied a high level of integration and the leveraging of new technologies.

- *Software compatible*

  Any new graphics system had to be compatible with the large set of libraries with graphics software already written, and must transparently accelerate software written to existing APIs.

Creator3D Graphics

Creator3D framebuffers are standard on all Ultra 2 systems. Combined with the UltraSPARC-II CPU and the UPA interconnect, Creator3D Graphics delivers outstanding window system, geometry, and imaging acceleration. Creator3D framebuffers contain 15 MB of video memory to support double-buffered operation and the acceleration of 3D applications or fast animation in 2D and 3D. Other features include:

- Full performance, low cost, 24-bit true color standard
- Transparent acceleration for X11, XIL, XGL, and OpenGL graphics libraries
- Common frame buffer and register architecture
- 8-bit X11 visuals supported include pseudocolor (default), linear / nonlinear greyscale, direct color
- 24-bit X11 visuals supported include direct color, linear / nonlinear truecolor
- 8-bit pseudocolor overlays
- High resolution (1920 x 1200 and 1280 x 900 in single buffer mode)
- Stereo ready
- On-board YCC to RGB color space conversion for fast video decompression
- Full 3D solids, dynamic shading, rotation, and Z-buffering acceleration
- Full double-buffered 24-bit true color, 8-bit overlay, 28-bit Z-buffer, 4-bit stencil

Creator Graphics Theory of Operation

Because the decision had been made to develop the graphics subsystem as part of the overall Ultra architecture, it was possible for engineers to place components in the new system where it would be most beneficial to graphics performance. Such placement minimizes overhead and ensures best possible

utilization of bus bandwidths and investments in ASIC technology, resulting in a very highly-integrated, economical, modular architecture that is tightly coupled the CPU, memory interconnect, frame buffer, and graphics accelerator (figure 4-1).

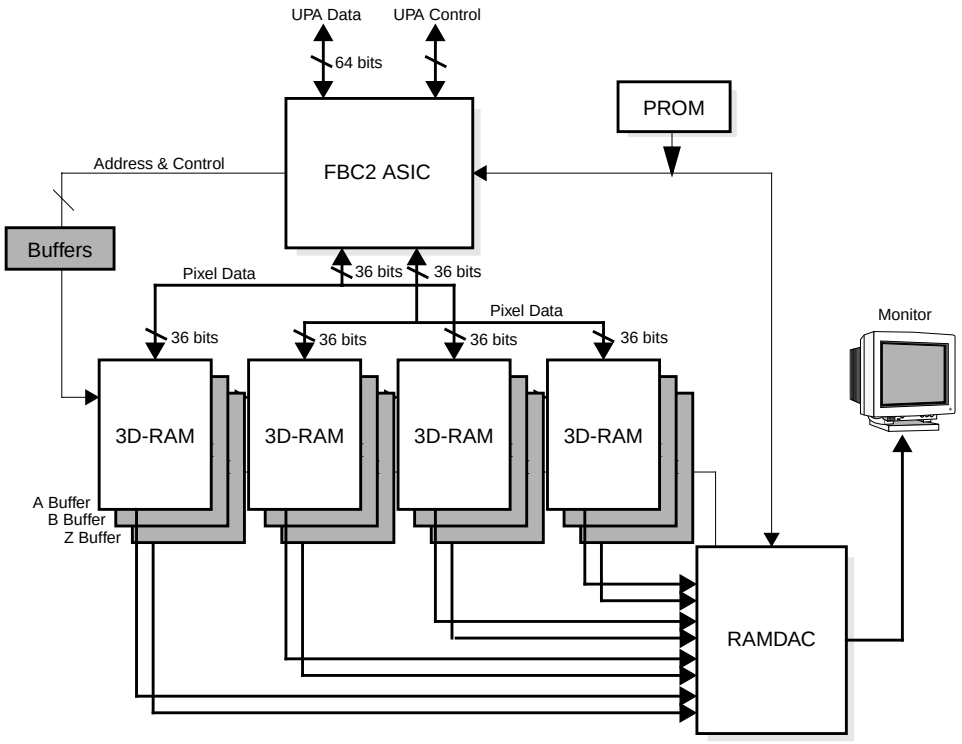

Figure 4-1 Ultra 2 systems equipped with Creator Graphics use a very highly-integrated, modular architecture that tightly couples the CPU, the system memory interconnect, the frame buffer, and graphics accelerator technology

In the Ultra 2 Creator models, graphics processing is spread out across the system to take advantage of appropriate resources: the UltraSPARC-II processor provides fast, scalable image and video processing; the Creator3D Graphics module accelerates the window system and 2D graphics; and both work together to accelerate pipelined 3D graphics instructions.

With large amounts of image and graphics data moving between processor, memory, and the Creator3D Graphics system, the UPA interconnect is essential to achieving high graphics performance. Its use of independent address busses, deep pipelining, and burst transfers make this possible.

Elite Graphics

Elite3D m6 is Sun's highest performance graphics subsystem. Elite3D-equipped systems are designed to help accelerate applications that manipulate large numbers of complex 3D solids and for use in MCAD, geotechnical, animation, or related fields. Elite3D dramatically improves performance in double-buffering, triangle and quad rendering, and lighting and shading without sacrificing fast 8- and 24-bit window system, imaging, or video performance.

Elite3D systems provide 88 bit planes, including full 24-bit double-buffer planes as required for smooth animation. A 28-bit Z-buffer is included to provide hardware assistance for hidden surface removal and dynamic rendering of 3D objects. Elite3D is fully upward compatible with Sun's Creator3D systems and does not compromise window system, 2D graphics, imaging, or video performance.

Elite3D features include:

- Simultaneous 8-bit and 24-bit visual support
- Multiple hardware colormaps
- Adjustable gamma correction
- 8-bit SOV-compliant pseudocolor overlay
- Transparent acceleration for X11 and XIL graphics libraries
- Transparent acceleration for 3D APIs (XGL, OpenGL, and Java3D APIs)
- 3D solids, dynamic shading, rotation, and Z-buffered acceleration
- Full double-buffered 24-bit true color, 8-bit overlay, 28-bit Z-buffer (floating point), 4-bit stencil (with full support for OpenGL stencil functions)
- High resolution (1280 x 1024 @76Hz non-interlaced)
- Stereo-ready (single pass, 960 x 680 @112 Hz non-interlaced)
- DDC2B monitor serial communication with EDID support

The Ultra 2 workstation supports the Elite3D m6 framebuffer. With six high performance, on-board floating point processors, Elite3D m6 performance is as high as five times that of the Creator3D.

Elite3D also provides support for a range of important 2D and 3D functions described in Table 4-1.

Theory of Operation

The Elite3D graphics module is comprised of a number of specialized ASICs for interface and control (*AFB-Command*), floating point operations (*AFB-Float*), and pixel drawing (*AFB-Draw*). Like Creator3D, the Elite3D graphics module uses twelve 3D-RAM chips to provide a 1280 x 1024 double-buffered 24-bit frame buffer with a 28-bit depth buffer. Elite3D and Creator also share the same Bt498+ RAMDAC (Figure 4-2). To avoid difficulties implementing switched bidirectional buses at 120 MHz, the Elite3D design uses unidirectional point-to-point buses for all three of its internal high speed buses. One of the busses (*FD-Bus*) runs at 800 MB per second.

2D Operations	3D Operations	Other Features
• *Bresenham lines*	• *Accelerated dots, lines, triangles, and quads*	• *Viewport clipping*
• *Polygons*	• *Hardware antialiasing of dots and lines*	• *Window ID clipping*
• *Font support*	• *Hardware support of large antialiased dots up to 10 pixels in diameter*	• *Hardware line patterning for all lines*
• *Rectangle fill*	• *Gouraud shaded triangles*	• *32 x 32 area pattern*
• *Fast block clear*	• *Specular lighting*	• *Flexible blending operations*
	• *Hardware per-pixel depth-cue*	• *Full set of Boolean operations*
	• *Hardware transparency (both alpha-blended and screen-door)*	• *Stateless frame buffer available in both 8 and 24 bits*
	• *Alpha interpolation per pixel*	• *Full plane mask*
	• *Texture map support*	
	• *Compressed 3D geometry decompression*	

Table 4-1 Functionality supported by the Elite3D graphics accelerator

The *AFB-Command* ASIC buffers and converts incoming 3D geometric data to independent primitives (triangles, lines, dots) which are then distributed to the six floating-point chips for further processing. In addition to the regular data input functions, AFB-Command has a decompression unit capable of converting highly compressed 3D geometric data back into the standard formats required by the rest of the graphics pipeline. Software APIs like

Java3D provide for geometry compression. The AFB-Command chip also permits the efficient reading and writing of pixels to and from the frame buffer memory.

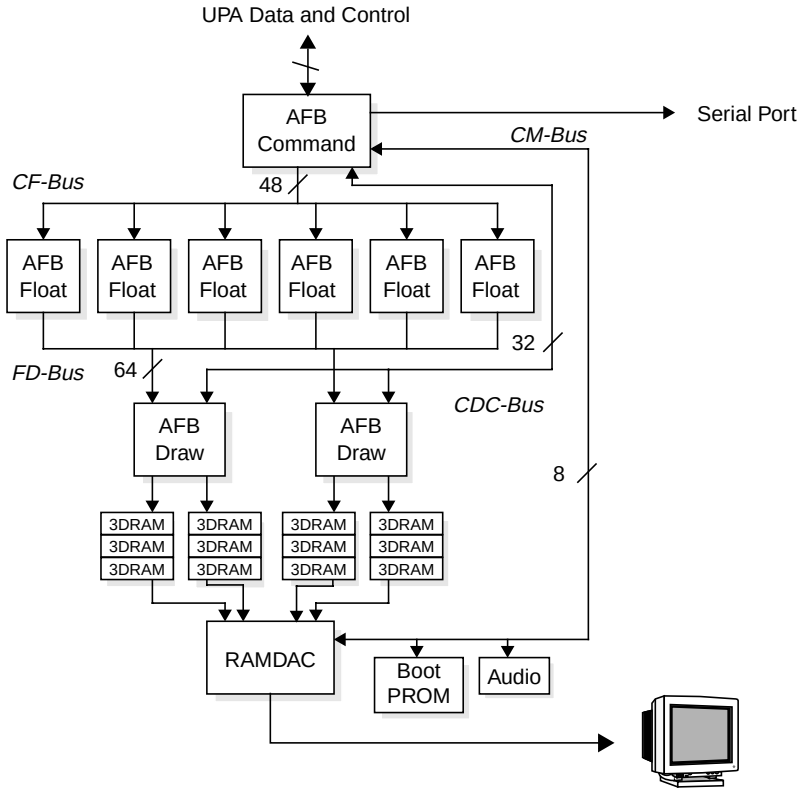

Figure 4-2 The Elite3D M6 graphics accelerator

The *AFB-Float* components are designed to transform, light, clip, and set up primitives which are passed to it from the AFB-Command chip. Six floating point units are used on the Elite3D m6. This module enhances performance by providing algorithm-specific circuits dedicated to just one (or a few) stage(s) of the graphics pipeline.

AFB-Draw takes in screen-space (fully transformed and lit) primitives and renders them into the frame buffer, drawing dots, lines and triangles as efficiently as possible. It also performs optional antialiasing on dots and lines. AFB-Draw contains edge walking and span interpolation circuitry to render individual pixels.

Other functionality includes:

- Single-pixel dots, antialiased dots, and large antialiased dots
- X11 Bresenham lines
- X11 Bresenham edge 2D polygons
- DDA lines and antialiased DDA lines
- DDA Gouraud interpolated triangles
- DDA triangles with texture mapping
- Screen aligned rectangular patterned fills and vertical scrolls
- Fonts (stencil)

Support is also included on a per pixel basis for:

- Alpha channel blend/transparency
- Screen door transparency
- Depth cueing
- Write-masks
- WIDs (Window IDs)

Key to Elite3D's performance is the rate at which AFB-Draw can render 24-bit depth-cued pixels into the 3D-RAM based frame buffer — nearly 400 million pixels per second. To achieve these high rates, the 3D-RAM is four-way interleaved, with two AFB-Draw ASICs to control two interleaves each.

AFB-Draw also handles all pixel operations such as blending, depth-cuing, boolean operations, bit masks, fonts, window-ID clipping, viewport clipping, and so forth. There is logic in the chip to allow "direct port" accesses to slip in between "accelerator port" access as needed. AFB-Draw also supports frame buffer read operations over the UPA interconnect.

4

Other Key Graphics Technologies in the Ultra 2

Much of the success of both the Creator3D and Elite3D graphics systems can be traced to the high level of integration throughout the design of the Ultra 2. While each frame buffer relies on innovative engineering and sophisticated components to achieve high performance, other components of the Ultra 2 make critical contributions.

The UltraSPARC-II Microprocessor

Until recently a system like Ultra 2 would have been impossible to build. Only with new advances in processor technology have CPUs been available with the necessary processing power to drive such a system. By using fast general purpose CPUs like UltraSPARC-II, it has finally become possible to build inexpensive systems that provide high-end 3D performance.

UltraSPARC's capacity for handling large numbers of high-speed floating-point calculations enables it to accelerate part of the 3D graphics pipeline calculations in Creator3D systems. (The Elite3D has up to six of its own floating point units for maximum performance.)

In Ultra 2 systems, image processing is also handled by the CPU, an approach with many advantages:

- *Better performance in memory-intensive tasks*

  When processing is done in the CPU, images can be held in system memory. Because many image processing algorithms operate on neighboring pixels, the system cache and MMU can help to dramatically speed up these functions.

- *Scalable performance*

  By giving image processing operations to the CPU, scalability can be achieved by adding faster or larger numbers of processors to the system. Many image processing functions can also benefit from parallel execution on multiprocessor machines.

- *Faster rendering*

  Most image processing is performed in a pipelined fashion with the results of one operation serving as the input image for another, with only the final image being displayed to the screen. With the Elite and Creator graphics

systems, these intermediate images can be written to fast system memory. When the final image is ready, it can be cropped, panned, zoomed, and copied to the screen via a fast block copy.

- *Exploitation of the UltraSPARC-II VIS Instruction Set*

  The UltraSPARC-II VIS Instruction Set allows the CPU to directly access and operate on image (pixel) data with a high degree of parallelism. Other instructions are also available to format and move data at a high rate of speed. Still others can aid with volume rendering and video compression and decompression.

The UPA Interconnect

Imaging, multimedia, and video applications all place large demands on system architectures. Furthermore, the design goal to make 24-bit graphics a standard feature on high performance Ultra systems places additional stress on interconnect performance—three times the pixel data must travel through the system when dealing with 24-bit data rather than 8-bit data. Because most imaging and video operations are performed in the UltraSPARC-II CPU in the Elite3D and Creator3D graphics systems, a high performance path is needed for image data to move between the CPU, memory, and frame buffer.

3D graphics applications can also be slowed if the flow of graphics commands fails to keep the pipeline of the graphics device full. Because the first portion of the 3D graphics pipeline uses the UltraSPARC's floating point units in the Creator3D systems, the need for a high-bandwidth path between the CPU and the frame buffer was further underscored.

The UPA interconnect, with its 64-bit data path to the graphics subsystem, can move data at the required high speeds between the CPU, memory, and graphics systems, providing much greater throughput than previous MBus-based systems in commonly encountered, real-world situations.

Software 5

The Solaris™ Operating Environment

The Ultra 2 supports Sun's latest version of the Solaris operating environment, Solaris 7, as well as Solaris 2.6 (3/99), and Solaris 2.5.1 (11/97). Solaris 7 includes a proven, scalable 32- and 64-bit kernel, standards-based networking, and Java technology support. These technologies provide the foundation for building and deploying enterprise-class systems for multi-vendor, multi-client workgroup environments, as well as highly available data center environments. The strengths of Solaris lie in its enterprise-class reliability, scalability, and performance. Solaris 7extends, and expands upon, these strengths.

Solaris 7 is a 64-bit kernel that provides enhancements in overall performance, scalability, reliability, availability, security, and ease-of-use while maintaining backward compatibility for all existing 32-bit Solaris applications. Solaris 7 continues the tradition of providing exceptional functionality and performance by delivering the following major enhancements:

- *Mainframe-class reliability, availability, and serviceability* for systems of all sizes
- *Higher performance*, the complete 64-bit computing environment provides greater capacity, precision, and performance
- *Enhanced scalability* with a 64-bit kernel that enables access to more system resources and the ability to consolidate applications onto a single server
- *Greater ease-of-use*, including Web-based installation, text and voice notes, and a graphical process manager

- *Comprehensive global support*, including support for the Euro currency symbol, complex text formats for Arabic, Thai, and Hebrew languages, and support for the development of multilingual applications
- *Software investment protection* with complete binary compatibility that ensures all of today's 32-bit Solaris applications continue to run on Solaris 7 without modification
- *Extended security features* through authentication, data integrity, data privacy, and single sign-on capabilities so that tampering, snooping, and eavesdropping do not compromise data or associated transactions
- *Year 2000 compliance*, ensuring no errors result when moving from date 12/31/99 to 1/1/00 or from 2/29/00 to 3/1/00
- *32-bit and 64-bit development environment*, enabling developers to generate a single set of source code that runs on both operating modes

Designed to deliver the power, flexibility, availability, and compatibility to support enterprise-wide computing, Solaris 7 combines four key computing elements — operating system, networking, window system, and user environment — into a stable, high-quality foundation that enables the development, delivery, and management of a wide range of computing solutions.

Operating System

Based on UNIX System V Version 4 (SVR4), Solaris provides a rich applications development environment, and fully supports symmetric multiprocessing (SMP) and multithreaded applications on multiprocessor machines. Solaris ensures maximum portability across platforms by conforming to several important standards including SPARC ABI, CDE-compliant Motif, X11R6, POSIX 1003.1b and 1003.2, NIS, WebNFS™, HTTP, IIOP, UNIX 95 and UNIX 98 branding, X/Open (XPG4 base functionality), EPA Energy Star, Kodak Color Management System, and ISO 9660.

Networking

Sun's Open Network Computing (ONC+) enables transparent access to information and services distributed throughout the environment. Solaris also defines a standard interface to ONC+ for alternative networking technologies (DCE and NetWare) enabling smooth integration with enterprise computing environments. Networking products such as NIS+, NFS, and RPC/XDR are

supported for remote execution and data exchange. Transport layer independence ensures support for a variety of network transport protocols such as TCP/IP (figure 5-1).

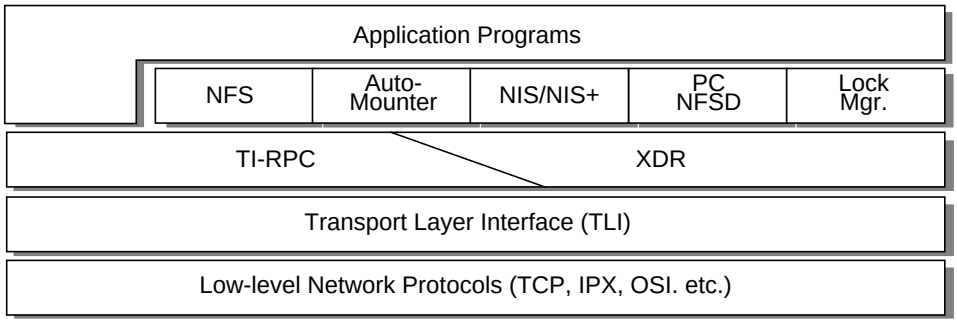

Figure 5-1 Solaris supports a family of advanced networking protocols and services.

Windowing Systems

The Solaris X11-based window server, user interface, and ToolTalk™ messaging services are engineered to exploit the Solaris distributed client-server computing model. To ensure a consistent look and feel across all major UNIX platforms, Sun includes the Common Desktop Environment (CDE) with every copy of Solaris. Now users and developers will have the choice of continuing to use the Sun OpenWindows environment, or the Motif-based industry standard, CDE. The CDE environment includes graphics, imaging, audio and video services, and Display PostScript to facilitate the development and delivery of multimedia applications for communication and collaboration across the enterprise.

Solaris 7 supports numerous graphics and windowing APIs such as XIL, XGL, Xlib, Display Postscript, and OpenGL to assist in the development of applications (figure 5-2). In addition, Solaris 7 includes Xlib and OpenGL 64-bit ready, high performance graphic APIs.

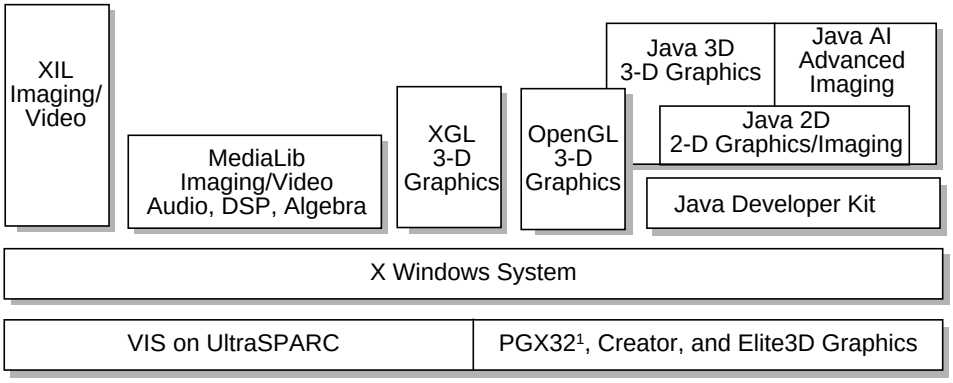

Figure 5-2 Solaris foundation graphics libraries and layered interfaces from Sun and other vendors.

CDE has been extended to include a variety of tools to simplify the management of applications and the desktop environment—a front panel to launch applications with a single click; a workspace manager to create multiple virtual desktops, including support for multiple monitors; a style manager to personalize the use of colors, backdrops, mouse and keyboard behavior, and startup characteristics. Other tools include text and icon editors, an image viewer, process and system management controls, workgroup calendaring, file and print manager, web-browser, performance meter, and MIME-compatible electronic mail. Solaris CDE features drag-and-drop and cut-and-paste across OpenWindows and Motif applications.

Installation

Solaris installation is fully automated using the Solaris JumpStart™ technology. When the system is first powered on, JumpStart software locates the install information over the network or from a local CD drive. The software installation is driven by profiles customized by the system administrator, or from a default installation profile, called the SmartStart™ profile. The SmartStart profile intelligently determines the best Solaris installation based on heuristics such as the amount of installed memory and available disk capacity.

Solaris Web Start eliminates the UNIX system administration chores normally associated with software deployment through a flexible software management console that can be run from any desktop in an organization's network. An easy to use tool for software deployment and management, Solaris Web Start is a Java application that simplifies and accelerates the installation of Solaris and associated software. A browser interface provides a familiar way to deploy and manage software resources in the workgroup and even across the Web. Customization and configuration options provide the flexibility needed for even the most unusual configurations, and by leveraging Sun's JumpStart technology, Solaris Web Start provides the advanced replicated installation and remote software deployment features demanded by enterprise administrators:

- One-button and custom deployment options simplify installation and configuration.
- Java management console looks like a set of web pages.
- Support for a variety of media, including CDROMs and the Web, enhances distribution options.
- Extensive context-sensitive and on-line documentation delivers help and support when needed.
- File system tools streamline the software installation process.
- Replicated installation “profiles” ease the enterprise administration burden.
- Remote option directs deployment from any desktop to any host.
- A Software Developers Kit (SDK) extends the benefits of Solaris Web Start to all developers of Solaris applications.

Support for Graphics Accelerators

Ultra systems support all of Sun’s Solaris 7 graphics APIs, including the XGL, XIL, and OpenGL libraries, Display PostScript, and the OpenWindows Version 3 (X11-compliant) window system. Industry-standard X-extension libraries, such as Xlib and PEXlib, are also available and are accelerated via the Sun foundation graphics libraries.

As both imaging and geometry devices, the graphics products available for Ultra systems accelerate many of the APIs mentioned above. The following sections briefly describe the foundation graphics interfaces and the functions accelerated by the Creator3D and Elite3D graphics subsystem.

OpenGL

The OpenGL graphics application programming interface is an industry-standard, vendor-neutral software interface which operates independently of operating and window system platforms. Based upon its proprietary predecessor, GL, OpenGL is an applications programming interface that provides 2D and 3D graphics functions, including modeling, transformations, color, lighting, and smooth shading, as well as advanced features such as texture mapping, NURBS, fog, alpha blending, and motion blur. The OpenGL API works in both immediate and non-editable display-list graphics modes.

The OpenGL library is targeted at developers creating interactive 3D applications for the enterprise, the intranet, and the Internet. These developers are generally affiliated with technical markets or in research facilities. Potential users include those in computer-aided design and manufacturing, global information systems, simulation, industrial design and modeling, entertainment, biochemistry, and petroleum exploration.

Sun™ OpenGL® for Solaris™ provides a complete solution for developing and deploying interactive 3D applications across Sun workstations. It enables mainstream, industry-leading 3D graphics and visualization applications to be deployed on Sun's Creator3D and Elite3D systems at a compelling price/performance ratio.

The widespread multivendor availability of OpenGL libraries ensures source code portability of 3D graphics clients. Open GL 1.1.2 for Solaris is a compliant implementation of OpenGL 1.1 from the OpenGL Architecture Review Board and is, therefore, source code compatible with other compliant OpenGL applications. Most existing OpenGL applications will only need to be recompiled in order to run under OpenGL 1.1.2 for Solaris.

OpenGL 1.1.2 for Solaris provides an implementation of OpenGL that incorporates hardware acceleration when used in conjunction with Sun Elite3D graphics:

- *Transformations - 2D (3x2) and 3D (4x4)*
- *Geometry Attributes - color, line type, fill pattern and textures, etc.*
- *Lighting and Shading - flat and Gouraud as well as up to 32 light sources (positional, directional, spot, and ambient)*
- *Non-Uniform Rational B-Splines (NURBS)*

- *Transparency - screen-door and alpha blended transparency*
- *Anti-Aliasing*
- *Depth Cueing - linear and scaled*
- *Texture Mapping - 2D texturing of 3D surfaces (accelerated using VIS)*

Specific OpenGL 1.1 extensions supported by Sun include:

- *3D texture mapping*
- *ABGR reverse-order color format*
- *Texture color table*
- *SGI color table*
- *Sun geometry compression*
- *Rescale normal*

Fully integrated with Solaris 7, OpenGL 1.1.2 allows developers to take advantage of it's advanced features, including multithreading and full support for 64-bit computing. OpenGL 1.1.2 also includes new imaging extensions to allow developers access to both graphics and imaging functionality within the same application and other enhancements to support increased performance and functionality. Solaris OpenGL can run with Common Desktop Environments (CDE) or OpenWindows environments. A defined common extension to the X Window System allows OpenGL client to run across distributed heterogeneous networks.

The XIL™ Imaging and Video Library

The XIL library is a foundation-level imaging interface providing the common functions required by many imaging and video applications. As a foundation software layer for imaging applications, the XIL library defines how imaging operations, such as display, image manipulation, and video compression and decompression, are carried out. Some of the functions available through XIL include:

- Pan, zoom, scale
- Flips, transformations
- Raster rotation
- Sharpen, blur, convolution
- Monadic and dyadic image operations
- Blend, composite

All XIL integer functions, whether they are 8, 16, or 32 bits, are accelerated by the Ultra 2 graphics subsystem through application of VIS instructions. Floating-point operations are handled by the UltraSPARC processor's integrated floating-point unit.

Because many image processing functions lend themselves to parallelism, XIL is both "MT Safe", and "MT Hot". MT Safe means that XIL can be used safely in programs which employ multithreading, while MT hot indicates that XIL uses multithreading to parallelize selected image processing functions automatically, greatly accelerating performance.

The XGL™ Geometry Library

The XGL library is a Solaris foundation geometry library providing the functionality and performance required by applications requiring geometry manipulation and display. The XGL library provides for optimization of 2-D and 3-D rendering, including high-quality lighting and shading, advanced primitives (such as NURBS and meshes, texture mapping, antialiasing, and transparency), and a flexible geometry pipeline. The XGL library includes sophisticated state-of-the-art features, such as dynamic tessellation of NURBS surfaces, as well as flexible pipelines for lighting and transformation.

Creator3D and Elite3D subsystems provides acceleration for many XGL functions:

- Transformations — 2-D (3x2) and 3-D (4x4)
- Geometry Attributes — color, line type, fill pattern and textures, etc.
- Lighting and Shading — flat and Gouraud as well as up to 32 light sources (positional, directional, spot, and ambient)
- Transparency — screen-door and alpha blended transparency
- Anti-Aliasing
- Depth Cueing — linear and scaled

Software Development Support

Workshop Products

Successful application development requires that programmers have high performance compilers and tools. The Sun WorkShop family of products includes highly optimizing, automatically parallelizing compilers (versions of

Workshop are available that support the Fortran, C, and C++ programming languages); libraries of highly optimized routines; and tools to help analyze and tune code for additional runtime performance. Workshop features include:

- Integrated programming environment
- Motif user interface, providing a standard look and feel
- Tight, editor-centric tool integration
- Hyperlinks, enabling easy tool navigation
- Multiprocessing, multithreaded development tools
- Distributed and parallel make utilities
- Incremental linker, for faster builds
- Fix and Continue, enabling defects to be found and fixed quickly
- AppGuru, enabling very fast application development for C++
- New version of Rogue Wave Tools.h++ 7.0 class library
- Motif, Windows, and Java GUI Builder, for cross-platform development
- WorkShop Visual, enabling quick and easy GUI development
- GUI capture and testing, providing reverse engineering capabilities
- Three dimensional data visualizer, speeding debugging of complex arrays
- WorkSets and PickLists, facilitating quick access to work sessions
- WorkShop TeamWare, for source code and configuration management
- Extensive on-line manuals and help system

Of particular interest to developers is the ability of Workshop to perform several advanced optimizations that can speed applications performance:

- *Instruction scheduling*, to arrange the order in which instructions are executed and make optimal use of available machine resources.
- *Profile feedback*, to obtain frequency information about a program. The program is executed and the frequency information is applied to optimizations such as code motion and inlining.
- *Loop parallelization*, to rearrange loop code so that multiple processors may be work in parallel to complete the loop.
- *Cache blocking*, to rearrange loop code to make maximum use of the processor cache.
- *Loop inversion*, to reverse the order of nested loops to gain the advantages of improved loop parallelization or better cache blocking.

To take advantage of innovative UltraSPARC processor features, Sun Workshop compilers support both traditional and hybrid versions of the SPARC Version 9 architecture. Full 64-bit computing is available with SPARC

V9 support. A hybrid version, called V8+, precludes the use of all V9 64-bit addressing instructions, ensuring 32-bit compatibility with existing versions of Solaris and with other existing applications, while still allowing access to most of UltraSPARC's advanced capabilities, including the VIS instruction set.

Java Applications Development

A discussion of software development would not be complete without mentioning Java. Taking the industry by storm, Java promises true platform-independent software development for a large number of applications. Software developers have instantly recognized the potential of Java applications, with thousands of firms currently developing, or planning to develop Java-based products. Sun, the original developer of Java, offers software developers a unique opportunity with a comprehensive product line designed to streamline Java development.

The object-oriented Java platform delivers the benefits of reusable code, reduced cost of ownership, and broad integration, with the complex, heavyweight object housekeeping process required by other object-oriented development models. Sun’s family of Java APIs and development products, including Java WorkShop, the Java 2 SDK, and Java Studio, empower developers to create an entire new class of applications that truly enable network-based computing. Sun Ultra workstations are ideal platforms for these tools, permitting the development of both client and server components of Java solutions. Products can then be easily deployed to more powerful Sun Java Web servers or JavaStation™ client systems.

Bundled with Solaris 7 is the Java 2 Software Development Kit. The Java 2 SDK provides both essential development tools required for creating Java applications and a high-performance, scalable runtime environment that reliably delivers the faster execution of Java applications. Designed to deliver superior performance and scalability across the enterprise, applications developers recognize that the runtime system in Java 2 for Solaris sets a new standard for Java technology performance and reliability.

Open Firmware

Ultra supports the use of a standardized PROM-resident monitor program that is written in a special threaded-interpretive language. Called Open Firmware, this monitor is conformant to the IEEE 1275-1994 standard, also known as

Standard for Boot (Initialization Configuration) Firmware. Open Firmware can be brought up during the power-on process if a problem is encountered, or by executing a system *shutdown* followed by a level 0 *init*.

Once the Open Firmware monitor has control, a variety of diagnostics are available for key subsystems and peripherals:

- Video graphics
- SCSI interface logic on the system board
- Ethernet interface and AUI
- Internal and external disk drives
- Tape, diskette, and CD-ROM drives
- Serial ports
- Keyboard
- Memory

The Open Firmware monitor also provides tools to allow the continuous monitoring of the network and selective probing of devices on the SCSI bus.

Boot-time behavior and some diagnostics in Ultra80 systems are controlled through 1 MB of flash PROM. The use of flash PROMs permit the reprogramming of specific code blocks to implement updates and enhancements without requiring physical access to the PROMs. Reprogramming may be done from a CD-ROM located in the system or remotely by a system administrator over a local area network.

Diagnostics

The Ultra 2 platform has been designed for easy diagnosis and problem repair. Supporting this are several PROM-resident and UNIX- based diagnostic programs that can be applied by end-users and service personnel.

Power-On Self-Test (POST)

Under user control, a power-on self-test (POST) can be automatically executed to test the system board, NVRAM, on-board I/O devices, and memory system each time power is applied to the system. While not intended to be a comprehensive diagnostic, POST can quickly establish that no severe problems exist with the system, and communicates that through a set of light-emitting diodes (LEDs) on the keyboard. POST tests may be monitored via a serial-port connection to another desktop system or dumb terminal.

SunVTS™

The *SunVTS* system exerciser is a graphically-oriented UNIX application that permits the continuous exercising of system resources and internal and external peripheral equipment. Used to determine if the system is functioning properly, SunVTS incorporates a multi-functional stress test of the system through operating system level calls, and allows the addition of new tests as they become available.

References

Sun Microsystems Computer Company posts product information in the form of data sheets, specifications, and white papers on its Internet World Wide Web home page at: *http://www.sun.com*.

Look for the these and other Sun technology white papers:

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