The OpenPA Project

First Edition

Paul Weissmann

Berlin

Preface

This is the *dead-tree*, made-for-printing edition of **The OpenPA Project** (openpa.net). The content is based on the online version's content from mid-June 2006, parts and pieces were removed and modified for a sane print-out version.

 The OpenPA Project is an independent resource for information on PA-RISC based computers from HP and other vendors. **This project is independent of and does not represent The Hewlett Packard Company in any way.**

This is the first prerelease edition and may still contain contentual and typographical errors, which hopefully will be corrected in a next edition. Moreover we still have plans for a larger restructuring and expansion for the content for the print edition, which we also hope to include in the next edition, which is *very optimistically* slated for 2007. Besides adding more and polishing the content we have the dim hope of improving and fleshing out the print/conversion infrastructure, since there still remain several rough XSLT and TEXedges.

Set with LATEX.

Thanks

Many people helped The OpenPA Project with contributions and support over the years. Thanks go to:

- Bill Bradford, for hosting the project's site in its early days
- Frank McConnell, for the HP 9000/500 and FOCUS information
- Götz Hoffart, for the CSS/HTML help and inspiration
- Grant Grundler, for his continuing support
- Michael Piotrowski, for corrections and HP-UX background information
- Michael Shalayeff, for hosting the project's site and providing PA-RISC wisdom
- Ti Kan, for the technical explanations on the Stratus architecture

Contents

Chapter 1

Introduction

The OpenPA Project's primary goal is to provide an informational resource on the underlying microarchitecture, the hardware parts of PA-RISC computer systems and the supported operating systems. The book is separated in three main parts: the first discusses the architectural and hardware aspects of PA-RISC computers, the second part gives an overview on the available operating systems while the third and last parts provides an in-depth listing of the various PA-RISC computer systems with detailed specifications.

The origins of this book lie in its online cousin, openpa.net, which itself started out in 1999, when the author got his first PA-RISC workstation and found almost no coherent information sources on the web. The latter fact bothered him a lot, since the other popular Unix/RISC-workstation families were thouroughly and well documented. Moreover, at that time many old HP 9000 systems were phased out in favor of shiny new Unix or NT servers resulting in the availability of a lot used PA-RISC systems. The author then spent a lot of time digging through various webpages and into the USENET looking for documentation on these systems. After having gathered a considerable amount of information, documentation and references he finally decided to compile this to a webpage and make it publically available, which resulted in parisc.workstations.org, the first version of this site, hosted by Bill Bradford of SunHELP. Over the years more PA-RISC computers fell into his hands and he explored other available operating systems, resulting in many more details on this site. The support from HP for the PA-RISC-Linux Project made more interesting documents about PA-RISC internals available. Furthermore, other open-source operating systems for PA-RISC computers made significant progress so these computers were used by an increasing amount of people. Several moons later, the site got renamed to openpa.net (around 2001) and soon moved to its own hosting facility. Plans for an offline-viewable edition suited for printing-out came up first in 2002, but were soon abandoned for lack of technical feasibility. A second attempt was started in the beginning of 2006, which then lead to the successful implementation of a useable dead-tree edition. The way from the online sources to this PDF is quite long, but it worked out in the end; the bulk of the process is automated, the only truly handrolled parts are this introductory chapter and the main TEX file.

Chapter 2

PA-RISC Hardware Details

2.1 PA-RISC Processors

2.1.1 Introduction

The PA-RISC architecture was the offspring of previous design efforts and lessons that HP learned from developing the FOCUS CPU, the world's first full 32-bit microprocessor. The FOCUS CPU was at its time (pre-1984) a huge chip (about 450.000 FETs) with a stack-based instruction set. There is a detailed description of the FOCUS architecture on the HP 9000/520 page.

The PA-RISC processors were designated to replace the old 16-bit stack-based CPUs in HP 3000 servers and the Motorola 680x0 CPUs in HP's UNIX workstations and servers. The overall design was quite conservatively RISC:

- the instruction set is implemented in hardware and not microcoded, opposed to several kinds of CISCs.
- the instruction size has a fixed length: one word (32 bit).
- only 3 addressing modes: long/short displacement and indexed mode.
- only load/store operation access the memory, no computational instructions directly access the memory.
- the PA-RISC instruction set was designed to be a good target for optimizing compilers. Many simple, frequently used instructions execute in just one cycle, more complex computation were assigned to assist processors or software algorithms.

PA-RISC is a canonical load-store architecture with a 5-stage pipeline with hardware-interlocks from the beginning. The original PA-RISC 1.0 architecture included a single instruction/data bus, it later on moved to a "Harvard"-style architecture, featuring seperate instruction and data buses. It has thirty-two 32-bit integer general purpose registers (GR0-GR31), seven shadow registers (SR0-SR6) for fast-interrupts and thirty-two 64-bit Floating Point registers for the FPU, which also could be combined to 64 x 32-bit and 16 x 128-bit. The FPU is able to execute a Floating Point instruction simultaneously to the ALU. The original addressing was 48-bit wide, it was later on expanded to 64-bit (with the introduction of the PA-8000 line).

Compared to other RISC architectures from the time, the original PA-RISC design was quite unspectacular: it had typically fewer features than those but remained always at competitive speeds, especially in Floating Point areas. HP was the first to include multimedia extension in a commercially available microprocessor (MAX-1 in PA-7100LC and MAX-2 64-bit in PA-8000; see the separate Multimedia Acceleration eXtensions (MAX-1 and MAX-2) article.) which allowed vector operations on two or four 16-bit subwords in 32-bit or 64-bit integer registers.

2.1.2 Overview Table

CPU	ISA width	Clock max.	L1 Caches max.	L2 Caches max.	TLB	Super scalar	SMP	Units
PA-7000	32-bit	66MHz	256KB I 256KB D *off-chip*		96 I 96 D	1-way	No	1 Integer

PA-7100/ PA-7150	32-bit	125MHz	1MB I 2MB D *off-chip*		120	2-way	Yes	1 Integer 1 Floating Point
PA-7100LC	32-bit	100MHz	1KB I *on-chip*	2MB *off-chip*	64	2-way	No	2 Integer 1 Floating Point
PA-7200	32-bit	140MHz	2KB *on-chip*	1MB I 2MB D *off-chip*	120	2-way	Yes	2 Integer 1 Floating Point
PA-7300LC	32-bit	180MHz	64KB I 64KB D *on-chip*	8MB *off-chip*	96	2-way	No	2 Integer 1 Floating Point
PA-8000	64-bit	230MHz	1MB I 1MB D *off-chip*		96	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store
PA-8200	64-bit	300MHz	2MB I 2MB D *off-chip*		120	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store
PA-8500	64-bit	440MHz	512KB I 1MB D *on-chip*		160	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store
PA-8600	64-bit	550MHz	512KB I 1MB D *on-chip*		160	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store
PA-8700	64-bit	875MHz	768KB I 1.5MB D *on-chip*		240	4-way	Yes	4 Integer 4 Floating Point 2 Load/Store
PA-8800	64-bit	1GHz	1.5MB I 1.5MB D *on-chip*	32MB *off-chip*	480	8-way	Yes	8 Integer 8 Floating Point 4 Load/Store
PA-8900	64-bit	1.1GHz	1.5MB I 1.5MB D *on-chip*	64MB *off-chip*	480	8-way	Yes	8 Integer 8 Floating Point 4 Load/Store
Hitachi PA/50	32-bit	60MHz	8KB I 4KB D *on-chip*		32 I 64 D	1-way(?)	No(?)	1 Integer 1 Floating Point
Hitachi HARP-1	32-bit	150MHz	8KB I 16KB D *on-chip*	512KB I 512KB D *off-chip*	128 I 128 D	2-way	No(?)	1 Integer 1 Floating Point

2.1.3 PA-7000 (PCX-S) *(Cheetah)*

Used in

- 705/35
- 710/50
- 720/50
- 730/66
- 750/66
- F10, F20, F30
- G30
- H20, H30
- I30

Overview

This was the first PA 1.1 CPU implementation and saw its first uses in the first true PA-RISC workstations and later in some of the *Nova* servers. It still was a multi-chip implementation.

Details

- PA-RISC version 1.1a 32-bit
- needs external FPU
- 96/96 I/D TLB
- 4/4 I/D BTLB
- 32-bit bus to I cache 64-bit bus to D cache
- off-chip caches up to 256KB/256KB I/D
- Up to 66MHz frequency with 5.0V core voltage
- 14.2 x 14.2 mm2 die, 580'000 FETs, 1.0 micron, 2-layer CMOS

2.1.4 PA-7100/PA-7150 (PCX-T) *(Thunderbird)*

Used in

- 715/{33,50,75}
- 725/{50,75}
- 735/{99,125}
- 742i/50
- 745i/{50,100}
- 747i/{50,100}

- 755/{99,125}
- G40, G50, G60, G70
- H40, H50, H60, H70
- I40, I50, I60, I70
- T500, T520
- Convex SPP1000/{CD,XA}
- Stratus Continuum 610S, 610, 615S, 615, 620, 625, 1220, 1225, 1245

Time of introduction

early 1992

Overview

The PA-7100 is a superscalar processor that is therefore able to issue more than one instruction at a time. It is the first PA-RISC CPU to integrate the ALU and FPU on a single die thus saving board space and lowering production cost. The communication channel between the PA-7100 and its instruction cache has been doubled which enables this CPU to achieve instruction level parallelism as described above. In this, multiple consecutive instructions are fetched by the CPU and simultaneously dispatched to independent integer and floating point units. The PA-7150 was basically the same as the 7100 with tweaks to the core and cache subsystem to allow clock frequencies up to 125MHz.

Details

- PA-RISC version 1.1b 32-bit
- 2 functional units: 1 integer ALU, 1 Floating Point unit
- 2-way superscalar
- CPU, FPU, MMU and cache controller on one VLSI chip
- *pipeline store* technique for reduction of penalty for execution of any store to data cache
- *stall-on-use* mechanism for parallel procession of instruction streams and cache misses
- 3 instruction queue
- hardware TLB miss handler
- hardware static branch support
- I/D cache bypass *(7150)*
- off-chip L1 caches up to 1MB I and 2MB D realized in asynchronous standard SRAMs
- I/D caches are both 64-bit per access, direct mapped, parity protected and cycled at CPU clock
- caches are software accessible
- caches are virtually indexed and physically tagged to minimize latency

- 120-entry fully associative TLB
- 16-entry BTLB with programmable page sizes up to 64MB
- system speed interface speed programmable to 1.0, .67 and .50 processor speed
- dual precision floating point latency: 2 cycles at 100MHz, load-use penalty is one cycle, branch penalty 0 (predicted) and 1 cycle (mispredicted)
- two different MP connection strategies supported
- MP cache coherency support
- up to 100MHz frequency (PA-7100) with 5.0V core voltage
- up to 125MHz frequency (PA-7150) with 5.0V core voltage
- 14.0 x 14.0 mm2 die, 850'000 FETs, 0.8 micron, 3-layer metal CMOS packaged in a 504-pin ceramic PGA package
- power dissipation of 30W at 100MHz

2.1.5 PA-7100LC (PCX-L) *(Hummingbird)*

Used in

- 712/{60,80,100}
- 715/{64,80,100}
- 725/100
- 743i/{64,100}
- 748i/{64,100}
- D200, D210, D300, D310
- E25, E35, E45, E55
- Hitachi 3050RX 225, 235
- SAIC Galaxy 1100

Time of introduction

1994

Overview

The PA-7100LC was primarily designed as a single-chip solution for application in low cost systems while still delivering the performance of '91 high-end workstations and servers. Contrary to earlier PA-RISC version 1.1 implementations which needed several support chips for the MPU the PA-7100LC integrates the CPU, FPU, MIOC *(memory and I/O controller)* and a first-level cache on a single VLSI chip. Both CPU and FPU support the *PA-RISC 1.1 Edition 3 ISA*.

Details

- PA-RISC version 1.1c 32-bit
- 3 functional units: 2 integer ALUs, 1 Floating Point unit *(See Note 1)*
- 2-way superscalar
- DRAM-memory & cache controller (MIOC) integrated on die
- 1KB on-chip I L1 instruction cache, direct mapped, 64-bit per access, prefetch from off-chip I cache
- 8KB-2MB off-chip unified I/D L1 cache, direct mapped, hashed address, virtual index, 480-600MB/s bandwidth
- (the 1KB on-chip I cache is not really considered a true cache, thus the off-chip cache in fact is the system's real L1 cache.)
- 32-Byte cache line size
- support for bi-endian load-store operations
- MAX-1 multimedia extensions (subword arithmetic) for multimedia applications, e.g. MPEG decoding
- Floating Point load-store to I/O space
- 64-entry unified I/D TLB, fully associative, 4K page size
- 8-entry BTLB, page sizes from 512K - 64M
- 64-bit wide load/store operations
- I and D cache bypassing
- *stall on use* D cache miss policy
- *don't fill on miss* cache hint
- hardware TLB miss handler support
- hardware *static* branch prediction
- GSC bus interface
- 64-bit ECC interface to the main memory
- instruction line prefetch from main memory
- up to 100MHz clock
- not MP capable
- 14.2 x 14.2 mm2 die, 900'000 FETs, 0.75 micron, 3-layer aluminium process packaged in a 432-pin PGA

Notes

1. Only one of the two integer ALUs is able to handle loads, stores and shifts, these operations can only be paired with simple math operations, like integer addition or multiplication. Both units can handle branch operations.

References

- **PA7100LC ERS (External Reference Specification)**[1] (PDF, 410KB) Detailed official description of the PA-7100LC processor and its microarchitecture. Hewlett-Packard Company (1999).

2.1.6 PA-7200 (PCX-T') *(Thunderbird')*

Used in

- C100, C110
- D250, D260, D350, D360
- J200, J210
- K100, K200, K210, K220, K400, K410, K420
- Convex SPP1200/{CD,XA}
- Convex SPP1600/{CD,XA}

Time of introduction

early 1995

Overview

The PA-7200 is leveraged from the original PA-7100 design, big parts of the core were just shrunk for the new 0.55 micron process. The FPU was taken over completely unchanged, retaining the same latencies for addition and multiplication even at a higher clock rate. It also acquired the cache design, e.g. had (for the time) big off-chip caches clocked at full CPU speed (140MHz). This chip was aimed at high-performance general-purpose applications but also on specialized applications that used large working sets which could take advantage of the high-bandwidth bus interface.

Details

- PA-RISC version 1.1d 32-bit
- 3 functional units: 2 integer ALUs, 1 Floating Point
- 2-way superscalar
- FPU, MMU, cache controller integrated on die
- 2KB on-chip 'assist' L1 cache, fully associative, holds 64 32-Byte cache lines
- off-chip L1 caches up to 1MB I and 2MB D realized in asynchronous SRAMs with one cycle latency
- (the 2KB on-chip *assist* cache is not really considered a true cache, thus the off-chip cache is the system's de-facto L1 cache.)
- caches are 64-bit per access, direct mapped, parity protected and cycled at CPU speed

[1] http://ftp.parisc-linux.org/docs/chips/PCXL_ers.pdf

- caches are virtually indexed and physically tagged to minimize latency
- 120-entry fully associative TLB
- 16-entry BTLB
- hardware TLB miss support
- six predecode bits
- support for uncached memory pages
- bi-endian support
- system speed interface speed programmable to 1.0, 0.75 and .67 processor speed
- Runway system/memory bus, 64-bit wide, 120MHz, 960MB/s max. bandwidth
- glueless interface to the system bus for up to four-way SMP (four CPUs on same processor bus)
- can have up to six bus-transactions in progress at once
- up to 140MHz frequency with 4.4V core and 3.3V I/O voltage
- 14.0 x 15.0 mm2 die, 1'300'000 FETs, 0.55 micron, 3-layer metal CMOS packaged in a 540-pin ceramic PGA package
- power dissipation of 29W at 140MHz

References

- **Design of the HP PA 7200 CPU**[2] (PDF, 170KB) Overview on the PA-7200 internals and memory/cache architecture. Kenneth K. Chan et al (February 1996: Hewlett-Packard Journal).
- **A Different Kind of RISC**[3] PA-7200 general overview. Dick Pountain (August 1994: BYTE Journal).

2.1.7 PA-7300LC (PCX-L2) *(Velociraptor)*

Used in

- 744/{132L,165L}
- 745/132L, 745/165L
- 748/132L, 748/165L
- A180, A180C
- B132L, B132L+, B160L, B180L+
- C132L, C160L
- D220, D230, D320, D330
- RDI PrecisionBook 132, 160, 180
- Hitachi 3050RX 255, 355E, 365E

[2] http://ftp.parisc-linux.org/docs/whitepapers/pa7200_design.pdf
[3] http://www.byte.com/art/9408/sec11/art3.htm

Time of introduction

mid 1996

Overview

The PA-7300LC is the direct descendant of the PA-7100LC and likewise designed for low-cost systems. It is still a *PA-RISC 1.1 3rd Edition* 32-bit processor in contrast to the 64-bit PA-8000 which was introduced in the same timeframe. While still being very close to the original PA-7100LC design it has several important enhancements:

1. large on-chip L1 caches, opposedly to the small assist caches of the 7100LC and 7200
2. integrated L2 and DRAM controller
3. improved bus interface

The available process technologies made it possible to include a large L1 cache on the CPU die, which breaks a big HP tradition of off-chip L1 caches. The PA-7300LC was the last PA-RISC version 1.1 CPU, all later workstations and servers switched to processors based on the 64-bit PA-RISC 2.0.

- PA-RISC version 1.1e 32-bit
- 3 functional units: 2 integer ALUs, 1 Floating Point unit *(See Note 1)*
- 2-way superscalar
- 64KB/64KB I/D on-chip L1 caches, each two-way set associative, virtually indexed
- cache line size of 32 Byte
- caches have a 64-bit datapath to the execution units, 256-bit datapath to main memory
- optional unified I/D L2 off-chip cache, up to 8192KB
- no hashing for both I and D caches
- L2 cache is write-through, direct mapped, physically indexed and physically tagged
- instruction prefetch buffer moved from memory controller to L1 instruction cache, thus allowing prefetch hits without penalty
- on-chip MIOC memory controller
- 96-entry unified I/D TLB
- 8-entry BTLB
- 4-entry ILAB
- faster GSC bus interface *(GSC+)*
- either 64-bit or 128-bit datapath from execution units to the memory
- up to 180MHz frequency with 3.3V core voltage
- 15.3 x 17.0 mm2 die, 9’200’000 FETs, 0.5 micron, 4-layer metal CMOS packaged in a 464-pin ceramic PGA package

Notes

1. Only one of the two integer ALUs is able to handle loads, stores and shifts, these operations can only be paired with simple math operations, like integer addition o multiplication. Both units can handle branch operations.

References

- **PA7300LC ERS (External Reference Specification)**[4] (PDF, 716KB) Detailed official description of the PA-7300LC processor and its microarchitecture. Hewlett-Packard Company (1996).
- **The PA-7300LC: the first "System on a Chip"**[5] (archive.org mirror) Presentation prepared for Microprocessor Forum 1995 summarizing the PA-7300LC. Tom Meyer (1996).
- **The PA 7300LC Microprocessor: A Highly Integrated System on a Chip**[6] (PDF, 50KB). Shorter summary of the PA-7300LC's design objectives and goals. Terry W. Blanchard and Paul G. Tobin (June 1997: Hewlett-Packard Journal).

2.1.8 PA-8000 (PCX-U) *(Onyx)*

Used in

- C160, C180
- D270, D280, D370, D380
- J280, J282
- K250, K260, K450, K460
- R380
- T600
- Convex SPP2000 (S-Class)
- Stratus Continuum 628, 1228

Time of introduction

January 1996

Overview

The PA-8000 is the first chip to implement the 64-bit PA-RISC 2.0 architecture which includes many extensions to support 64-bit computing. This includes that all integer registers and functional units (ALU, shift/merge) have been widened to 64-bit, i.e. native 64-bit integer arithmetic. The flat virtual address space is 64-bit wide although most PA-RISC version 2.0 CPUs only support a physical address space of 40-bit. Other extensions include fast TLB insert instructions, memory prefetch instructions,

[4] http://ftp.parisc-linux.org/docs/chips/pcxl2_ers.pdf
[5] http://web.archive.org/web/20040214111649/http://www.cpus.hp.com/technical_references/101995wp.shtml
[6] http://ftp.parisc-linux.org/docs/whitepapers/pa7300lc_on_chip.pdf

support for variable sized pages, branch prediction hinting and FPMAC *(Floating Point Multiply Accumulate)* units. The instruction decode logic is not integrated with the functional units' pipeline logic. This architecture allows the chip to partially decode instructions well in advance of the instruction's actual execution by the functional unit(s).

A key feature of the PA-8000 is the IRB *(Instruction Reorder Buffer)*. Due to restrictions on compiler scheduling, the design team decided that the CPU should perform its own instruction scheduling. The IRB can store up to 28 computation and 28 load/store instructions; it tracks interdepencies between these instructions and allows execution as soon as the instructions are ready. Branch prediction outcomes are also tracked and due to re-scheduling the CPU can execute instructions past cache misses. The IRB is the key part in the OOO execution capabilty of the chip.

In short, the PA-8000 is a decoupled architecture with four-instruction dispatch and aggressive out-of-order *(OoO)* execution. It has additionally dual floating-point and dual load/store units, a large OOO dispatch window and, following a long HP tradition, no on-chip caches. The (large) primary caches have been kept off-chip to increase the amount of data that can be accessed in a single cycle. Although the latency of the caches is roughly two cycles this can be hidden with complete pipelining resulting practically in one access per cycle. Nothing in the design of this chip was leveraged from previous chip designs.

Details

- PA-RISC version 2.0 64-bit
- 10 functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- 4-way superscalar
- 2 address adders
- 96-entry fully-associative dual-ported TLB
- TLB miss penalty of 61 cycles
- 32-entry BTAC *(Branch Target Address Cache)*
- 256-entry BHT *(Branch History Table)*
- *dynamic* and *static* branch prediction modes
- off-chip L1 caches up to 1MB I and 1MB D, realized in synchronous 6.7ns (150MHz) late-write 1Mb SRAMs, one cycle latency
- caches are direct-mapped and dual-ported
- 56-entry instruction queue/reorder buffer *(IRB)*
- MAX-2 multimedia extensions (subword arithmetic) for multimedia applications, e.g. MPEG decoding
- each instruction includes five predecode bits
- bi-endian support

- Runway system/memory bus, 120MHz, 64-bit wide, featuring split transactions and glueless multiprocessing. Max. throughput of 960MB/s
- Up to 180MHz frequency with 3.3V core voltage
- 17.7 x 19.6 mm2 die, 4'500'000 FETs, 0.5 micron, 5-layer metal CMOS packaged in a 1,085-pin flip-chip LGA package

References

- **Advanced Performance features of the 64-bit PA-8000**[7] (archive.org mirror) Detailed description of the PA-8000 innards, presented at CompCon 95. Doug Hunt (1995: IEEE CS Press). [Article reprint for vanished cpus.hp.com]
- **PA-8000 Combines Complexity and Speed**[8] (archive.org mirror More general introduction to the PA-8000. Linley Gwennap (1994: Microprocessor Report, Volume 8 Number 15). [Article reprint for vanished cpus.hp.com]
- **Four-Way Superscalar PA-RISC Processors**[9] (PDF, 190KB) Overview on PA-8000 and its sucessor PA-8200 with an eye on their execution capabilities. Anne P. Scott et al (August 1997: Hewlett-Packard Journal).

2.1.9 PA-8200 (PCX-U+) *(Vulcan)*

Used in

- C200, C240
- D390
- J2240
- K370, K380, K570, K580
- R390
- V2200, V2250

Time of introduction

May 1997

Overview

Shortly after the introduction of the PA-8000 the design team noted several aspects of this chip for improvement in the successor:

- branch prediction
- TLB miss rates

[7] http://web.archive.org/web/20040214092531/http://www.cpus.hp.com/technical_references/advperf.shtml
[8] http://web.archive.org/web/20040214122429/http://www.cpus.hp.com/technical_references/111994ar.shtml
[9] http://ftp.parisc-linux.org/docs/whitepapers/four_way_superscalar.pdf

- cache sizes

The new chip should offer improved performace, compatibility with existing applications and short time to market. The whole design should be heavily leveraged from the existing PA-8000 design foundation. The availability of new 4Mb SRAMs with faster access times allowed an increased CPU clockspeed and a bigger cache size. Furthermore the team analyzed that the PA-8200 performance could be enhanced significantly if "wasted cycles" while waiting for instructions and data were reduced. Due to this, it was concluded that increasing the BHT, TLB and caches are "high benefit, low risk" improvements.

Details

- PA-RISC version 2.0 64-bit
- 10 functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- 4-way superscalar
- 2 address adders
- 120-entry fully-associative dual-ported TLB
- 42-entry BTAC *(Branch Target Address Cache)*
- 1024-entry BHT *(Branch History Table)*
- *dynamic* and *static* branch prediction modes
- off-chip L1 caches up to 2MB I and 2MB D, realized in synchronous 5ns (200MHz) late-write 4Mb SRAMs, one cycle latency
- caches are direct-mapped and dual-ported
- 56-entry instruction queue/reorder buffer *(IRB)*
- each instruction includes five predecode bits
- MAX-2 multimedia extensions (subword arithmetic) for multimedia applications, e.g. MPEG decoding
- bi-endian support
- Runway system/memory bus, 120MHz, 64-bit wide, featuring split transactions and glueless multiprocessing. Max. throughput of 960MB/s
- Up to 300MHz frequency with 3.3V core voltage
- 17.7 x 19.6 mm2 die, 4'500'000 FETs, 0.5 micron, 5-layer metal CMOS packaged in a 1,085-pin flip-chip LGA package

References

- **Four-Way Superscalar PA-RISC Processors**[10] (PDF, 190KB) Overview on PA-8000 and its predecessor PA-8200 with an eye on their execution capabilities. Anne P. Scott et al (August 1997:

[10] http://ftp.parisc-linux.org/docs/whitepapers/four_way_superscalar.pdf

Hewlett-Packard Journal).

- **HP Pumps Up PA-8x00 Family**[11] (archive.org mirror) Description and results of the improvements made in PA-8200 and PA-8500. Linley Gwennap (October 1994: Microprocessor Report, Volume 10 Number 14). [Article reprint for vanished cpu.hp.com]

2.1.10 PA-8500 (PCX-W) *(Vulcan)*

Used in

- A400-36, A400-44 (rp2400), A500-36, A500-44 (rp2450)
- B1000, B2000
- C360, C3000
- J5000, J7000
- L1000-36, L1000-44 (rp5400), L2000-36, L2000-44 (rp5450)
- N4000-36, N4000-44 (rp7400)
- V2500
- Stratus Continuum 419, 429, 616S, 616, 619, 629, 1219, 1229

Time of introduction

September 1998

Overview

The PA-8500 is a direct evolution of the PA-8000 and PA-8200 processors; the processing core was taken over incorporating only minor changes. However, for the first time in a PA-RISC CPU, a large L1 cache was integrated directly onto the CPU die, breaking with a long-standing HP tradition of keeping the L1 caches off-chip (although the two years older PA-7300LC processor already included an albeit smaller L1 cache on-chip). Some of the other improvements include bigger TLB and BHT. The PA-8500 is a full 64-bit chip and as such supports a flat 64-bit virtual address space, although only 40 physical address bits are used by the chip, corresponding to one Terabyte of directly addressable memory. Backward compatibility to older 32-bit PA-RISC CPUs is provided.

The big challenge in developing the PA-8500 was its huge on-chip cache. It had to fit onto the allocated die area and be able to keep up with the IRB. A similar cache design to that of its predecessors was used, although the RAM cells for the cache now sat directly on the die. The data cache is composed of 0.5MB banks, implemented with four 0.125MB arrays providing error correction. The data is organized in such way that either a full cache line can be addressed at once or four ways of associativity together. The instruction cache is implemented as one bank of 0.5MB four-way set associative pipelined cache, providing 128 bits of instruction plus pre-decode bits per cycle.

[11] http://web.archive.org/web/20040214112604/http://www.cpus.hp.com/technical_references/101996ar.shtml

As his predecessors the PA-8500 is able to execute instructions speculatively; the processor guesses the path of the ongoing instructions and executes them in this path. If the guess is found to be incorrect, the speculatively executed instructions are discarded. Speculative execution is aided by a branch prediction mechanism based on the branch history table (BHT).

Details

- PA-RISC version 2.0 64-bit
- 10 functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- 4-way superscalar
- 2 address adders
- 160-entry fully-associative dual-ported TLB
- 32-entry BTAC *(branch target address cache)*
- 2048-entry BHT *(branch history table)*
- *dynamic* and *static* branch prediction modes
- on-chip L1 caches 0.5MB I and 1MB D, each 4-way set associatve
- 32 or 64 Byte cache line size
- Supports up to 1 TB of physically addressable memory (40-bit physical addresses)
- 56-entry instruction queue/reorder buffer *(IRB)*
- MAX-2 multimedia extensions (subword arithmetic) for multimedia applications, e.g. MPEG decoding
- bi-endian support
- Runway system/memory bus, 125MHz, 64-bit, DDR *(double data rate)*, about 2GB/s peak bandwidth
- Up to 440MHz frequency with 2.0V core voltage
- 21.3 x 22.0 mm2 die, 140'000'000 FETs, 0.25 micron, 5-layer metal CMOS packaged in a 544-pin LGA package

References

- **HP Pumps Up PA-8x00 Family**[12] (archive.org mirror) Description and results of the improvements made in PA-8200 and PA-8500. Linley Gwennap (October 1994: Microprocessor Report, Volume 10 Number 14). [Article reprint for vanished cpu.hp.com]
- **A 500 MHz 1.5 MByte Cache with On-Chip CPU**[13] (PDF, 141KB) Slides of a presentation on the PA-8500 CPU. Jonathan Lachman and J. Michael Hill (1997: ISSCC).
- **PA-8500: The Continuing Evolution of the PA-8000 Family**[14] (archive.org mirror) Description of

[12] http://web.archive.org/web/20040214112604/http://www.cpus.hp.com/technical_references/101996ar.shtml
[13] http://ftp.parisc-linux.org/docs/whitepapers/isscc_cache_talk.pdf
[14] http://web.archive.org/web/20040214131135/http://www.cpus.hp.com/technical_references/8500.shtml

PA-8500 development and technical details. Gregg Lesartre and Doug Hunt (1997: Proceedings of CompCon, IEEE CS Press). [Article reprint for vanished cpu.hp.com]

2.1.11 PA-8600 (PCX-W+) *(Landshark)*

Used in

- A400-5X (rp2400), A500-5X (rp2450)
- B2000 (some), B2600
- C3600
- J5600, J6000, J7600
- L1000-5X (rp5400), L2000-5X (rp5450)
- L1500-5X (rp5430), L3000-5X (rp5470)
- N4000-5X (rp7400)
- V2600
- Superdome
- Stratus Continuum 439, 449, 651-2, 652-2, 1251-2, 1252-2

Time of introduction

January 2000

Overview

The PA-8600 basically was just a PA-8500 with minor modifications to make it fit onto a new manufacturing process in order to achieve higher clock speeds. One of the only real changes applied to the original design was a *quasi LRU replacement* policy for the instruction cache. Moreover, the interface to the Runway bus apparently was slightly modified, and the order of the bus transaction reworked.

Details

- PA-RISC version 2.0 64-bit
- 10 functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- 4-way superscalar
- 2 address adders
- 160-entry fully-associative dual-ported TLB
- 32-entry BTAC *(branch target address cache)*
- 2048-entry BHT *(branch history table)*
- *dynamic* and *static* branch prediction modes

- on-chip L1 caches 0.5MB I and 1MB D, each 4-way set associatve
- 32 or 64 Byte cache line size
- Supports up to 1 TB of physically addressable memory (40-bit physical addresses)
- 56-entry instruction queue/reorder buffer *(IRB)*
- MAX-2 multimedia extensions (subword arithmetic) for multimedia applications, e.g. MPEG decoding
- Quasi LRU replacement policy for the instruction cache
- bi-endian support
- Runway system/memory bus, 125MHz, 64-bit, DDR *(double data rate)*, about 2GB/s peak bandwidth
- Up to about 550MHz frequency with 2.0V core voltage
- 21.3 x 22.0 mm2 die, 140'000'000 FETs, 0.25 micron, 5-layer metal CMOS packaged in a 544-pin LGA package

2.1.12 PA-8700 (PCX-W2) *(Piranha)*

Used in

- A400-6X , A400-7X, A400-8X (rp2430), A500-6X, A500-7X, A500-8X (rp2470)
- C3650, C3700, C3750
- J6700
- L1000-7X, L1000-8X (rp5400), L2000-7X, L2000-8X (rp5450),
- L1500-6X, L1500-7X, L1500-8X (rp5430), L3000-6X, L3000-7X, L3000-8X (rp5470)
- N4000-6X, N4000-7X, N4000-8X (rp7400, rp7405, rp7410)
- Superdome
- rp7410

Time of introduction

August 2001

Overview

The PA-8700 is also basically just an enhanced and revamped PA-8500 core with some slight modifications. As all PA-8x00 CPUs before, it logically still is very close to the original PA-8000 core from 1997. All subsequent new CPUs from HP were based on this design and added several features and some slight modifications to it while retaining the basic PA-RISC version 2.0 core. The PA-8700 enhanced the on-chip L1 caches and the TLB significantly while switching to a new CMOS-process helped boosting the clock-frequency. The chip was at its time one of the largest available commercial CPUs and one of the first to be manufactured in a SOI (Silicon On Insulator) process. The PA-8700 was

manufactured by IBM, in contrast to the PA-8500 and PA-8600, which were fabbed by Intel, after HP gave up its processor fabs long time ago.

Details

- PA-RISC version 2.0 64-bit
- 10 functional units: 2 integer ALUs, 2 shift/merge units, 2 complete load/store pipelines, 2 Floating Point multiply/accumulate units, 2 Floating Point divide/square root units
- 4-way superscalar
- 2 address adders
- 240-entry fully-associative dual-ported TLB
- 32-entry BTAC *(branch target address cache)*
- 2048-entry BHT *(branch history table)*
- *dynamic* and *static* branch prediction modes
- 0.75MB I and 1.5MB D on-chip L1 caches, each 4-way set associatve, implemented in independent 0.75MB banks.
- 32 or 64 Byte cache line size
- Data cache prefetching
- Quasi LRU replacement policy for *both* the instruction and data cache.
- Supports up to 16 TB of physically addressable memory (44-bit physical addresses)
- 56-entry instruction queue/reorder buffer *(IRB)*
- MAX-2 multimedia extensions (subword arithmetic) for multimedia applications, e.g. MPEG decoding
- bi-endian support
- Support for hardware lock-stepping, i.e. operating multiple chips in parallel to detect faults
- Runway system/memory bus, 125MHz, 64-bit, DDR *(double data rate)*, about 2GB/s peak bandwidth
- Up to 750MHz (875MHz on the PA-8700**+**) frequency with 1.5V core voltage
- 16.0 x 19.0 mm2 die, 186'000'000 FETs, 0.18 micron, 7-layer Silicon-on-Insulator CMOS packaged in a 544-pin LGA package

References

- **A 900MHz 2.25MByte Cache with On Chip CPU**[15] (PDF, 119KB) Slides of a presentation on the PA-8700 CPU, centered on the CPUs cache subsystem. J. Michael Hill and Jonathan Lachman (2000: ISSCC).

[15] http://ftp.parisc-linux.org/docs/whitepapers/isscc_cache_talk_2.pdf

2.1.13 PA-8800 (PCX-?) *(Mako)*

Used in

- A400-9X (rp2430), A500-9X (rp2470)
- C8000
- L1000-9X (rp5400), L2000-9X (rp5450),
- L1500-9X (rp5430), L3000-9X (rp5470)
- N4000-9X (rp7400, rp7405, rp7410)
- rp3410-2, rp3440-4
- rp4410-4, rp4440-8
- rp7420
- rp8400, rp8410, rp8420
- Superdome

Time of introduction

2004

Overview

Mako was supposed to breathe fresh life in the PA-RISC line, though it had strong internal competition from the Itanium-line (based on much HP development) and as such wasn't really marketed. The PA-8800 integrates two PA-8700 cores onto a single die, adds a very large off-die L2 cache (though with a very significant bandwidth) onto the CPU module, enhances the clock frequency a bit further and uses the Itanium/McKinley processor/system bus. Most systems which could handle a PA-8800 use the HP zx1-chipset and could be hardware-upgraded to use Itanium-processors.

Details

- 0.75MB I and 0.75MB D on-chip L1 caches *per core*
- no data passing between the cores' L1 caches
- 32MB off-chip L2 cache, four-way associative, physically indexed and tagged
- L2 cache is shared between both CPU cores
- L2 cache controller is on-die
- L2 implemented in DDR-ESRAM, four 8MB chips, 300MHz clock, each 2.7GB/s bandwidth
- total >10GB/s L2 cache bandwidth
- 1MB SRAM tags for L2 cache
- ECC for L2 data and tags

- *Itanium 2/McKinley* processor bus, 200MHz clock ("double-pumped"), 128-bit datapath, 6.4GB/s bandwidth, data ECC-protected, signals parity
- Up to 1 GHz frequency with 1.5V core voltage
- 23.6 x 15.5 mm2 die, 300'000'000 FETs, 0.13 micron, 8-layer Silicon-on-Insulator CMOS (fabbed by IBM)

References

- **HP's Mako Processor**[16] (PDF, 1.4MB) Slides of a presentation on the PA-8800 CPU. David J. C. Johnson (2001: Microprocessor Forum).

2.1.14 PA-8900

Used in

- rp3410-2, rp3440-4
- rp4410-4, rp4440-8
- C8000

Time of introduction

2005

Overview

The PA-8900 basically is the same as a PA-8800 featuring a doubled L2 cache and a slightly higher clock frequency. It supposedly is the last processor of the PA-RISC family, no more new PA-8x00s will be released. Future systems integration will be based around Itanium-family chips, although since HP canned Itanium-based workstations it seems the PA-8900-powered C8000 workstation will be one of the last HP-UX workstations.

Information on the PA-8900 is generally scarce, it seems there was not much interest releasing many details on the inner workings and architecture, no whitepapers or more detailed articles could be found.

Details

- 0.75MB I and 0.75MB D on-chip L1 caches *per core*
- 64MB off-chip L2 cache, four-way associative, physically indexed and tagged
- ECC for L2 data and tags
- *Itanium 2/McKinley* processor bus, 200MHz clock ("double-pumped"), 128-bit datapath, 6.4GB/s bandwidth, data ECC-protected, signals parity
- 44 bit physical addressing
- 64 bit virtual addressing

[16] http://ftp.parisc-linux.org/docs/whitepapers/mako_mpf_2001.pdf

- 4 GB maximum page size
- Up to 1.1 GHz frequency
- 23.6 x 15.5 mm2 die, 317'000'000 FETs, 0.13 micron, 8-layer Silicon-on-Insulator CMOS (apparently fabbed by IBM)

References

- **Overview of the HP 9000 rp3410-2, rp3440-4, rp4410-4, and rp4440-8 Servers**[17] (PDF, 700KB) Technical Whitepaper from HP on new servers and the PA-8900 processor. Hewlett-Packard (2005).

2.1.15 Hitachi PA/50

Used in

- Hitachi 3050RX 100C, 200

Time of introduction

about 1993

Overview

The PA/50 was a PA-RISC version 1.1 compatible processor designed and manufactured by Hitachi. Two designs were developed: **M** and **L**, the latter being the lower-cost product. They were meant as personal workstation or high-end embedded controllers. Hitachi integrated a set of previously features not existing (at that time) in any PA-RISC CPU,e.g. on-chip caches, data-prefetching, a power-saving mode and SDRAM support.

Details

- PA-RISC version 1.1 32-bit
- Built-in, pipelined FPU
- L1 I: 8KB, 2-way set-associative, 32-byte blocks
- L1 D: 4KB, 2-way set-associative, 32-byte blocks, copy-back
- L1 caches are on-chip
- uncacheable memory (per page)
- TLB: I/D 32/64-entry, 2-way set, 4K-page, each +2 additional block entries
- BTLB (256KB-32MB)
- Seven 32-bit shadow registers for fast interrupts
- Data-prefetching

[17] http://h71028.www7.hp.com/ERC/downloads/5982-4172EN.pdf

- Non-blocking cache
- Power-saving mode, reducing frequency to 1/8
- Support for SDRAM
- PA/50L: Up to 33MHz frequency with 3.3V core voltage
- PA/50M: Up to 60MHz frequency with 5.0V core voltage
- 11.5 x 12.0 mm2 die, 1'280'000 FETs, 0.6 micron, 3-layer metal CMOS packaged in a 160-pin plastic QFP package

2.1.16 Hitachi HARP-1

Time of introduction

June 1994

Overview

The HARP-1 was a PA-RISC version 1.1 compatible CPU from Hitachi; apparently a larger, faster version than the above PA/50 (sadly not much information available).

Details

- PA-RISC version 1.1 32-bit
- Built-in, pipelined FPU
- 2-way superscalar
- L1 I: 8KB, 1-way set-associative, 32-byte blocks
- L1 D: 16KB, 2-way set-associative, 32-byte blocks, copy-back
- L1 caches are on-chip
- L2 I/D 512/512KB, off-chip
- TLB: I/D 128/128-entry, 1-way set
- Up to 150MHz frequency with 3.3V core voltage
- 16.2 x 16.5 mm2 die, 2'800'000 FETs, 0.6 micron, 3-layer aluminium + 1-layer tungsten BiCMOS

2.2 PA-RISC CPU architecture

2.2.1 Overview

More in-depth explanations of some technologies and features present in PA-RISC processors.

2.2.2 Floating Point Unit (FPU)

The *Floating Point Unit* is an assist processor logically added to a system to improve the performance on floating-point operations. The processor can be on a seperate chip (e.g. PA-7000) or integrated onto the central CPU die (all PA-RISC CPUs upwards). The FPU executes special floating point instruction to perform arithmetic on its own set of independent registers (*register file*) and to move data between its own registers and the system's lower memory hierarchy. The FPU execution stage is pipelined. All PA-RISC FPUs contain thirty-two 64-bit registers, which can also be used as sixty-four 32-bit registers and sixteen 128-bit registers.

2.2.3 Memory and I/O Controller (MIOC)

The *Memory and I/O Controller* in the PA-7100LC processor and PA-7300LC processor is the integration of both DRAM/cache controller and I/O-controller on the processor die. It is very similar on both CPUs, not much has been changed in the transition from 7100LC to 7300LC.

The integrated memory controller requires only buffers and DRAM modules to build up the complete memory subsystem. A wide range of programmable options is implemented:

- support for 4, 16, 64 and 256 Mbit modules
- support for both FPM and EDO DRAM
- data bus width of 64(72) or 128(144) bit
- optional SEDC error control
- up to 16 physical memory slots
- support for a wide range of core frequencies
- support for 3.3V and 5.0V DRAM

On the PA-7300LC the memory controller also includes the SLC (*Second Level Cache Controller*). It provides an *optional* L2 cache, ranging from 32KB to 8MB (on almost all systems with a PA-7300LC, 2MB of L2 was used). It shares the data bus with the DRAM subsystem, so it has the same width (64/128-bit) and same optional SEDC error control.

2.2.4 Transition Lookaside Buffer (TLB)

The *Translation Lookaside Buffer* is a hardware structure doing the virtual-to-physical memory-address translations. It takes virtual page numbers and returns the corresponding physical page number. The PA-7000 is the last PA-RISC processor to use seperate I/D TLBs, all later PA 1.1 and 2.0 CPUs use a combined TLB structure.

- PA-7000 - 96 I and 96 D entries
- PA-7100 - 120 combined entries
- PA-7100LC - 64 combined entries
- PA-7200 - 120 combined entries
- PA-7300LC - 96 combined entries
- PA-8000 - 96 combined entries
- PA-8200 (PCX-U+) - 120 combined entries
- PA-8500 (PCX-W) - 160 combined entries
- PA-8600 (PCX-W+) - 160 combined entries
- PA-8700 (PCX-W2) - 240 combined entries

Translation process

- *PA 1.1*: If a virtual address has to be translated to a physical address, the corresponding TLB is searched for an entry matching the Virtual Page number. If an entry is found, the 20-bit Physical Page number, delivered by the TLB, is concatenated with the original 12-bit page offset to the build up the 32-bit absolute physical address.

TLB miss handling implementations

- *hardware*: If the CPU implementation provides a hardware TLB miss handler, it attempts to find the virtual-to-physical translation in the *Page Table*. If successful, the translation and protection fields are inserted in the TLB. If not successful, an interruption occurs so the software miss handler can complete the translation.
- *software*: If software TLB miss handling is implemented, a TLB miss fault interruption routine performs the translation. It inserts the translation and protection fields in the TLB and afterwards restarts the interrupted routine, in which the TLB miss occurred.

2.2.5 Block Transition Lookaside Buffer (BTLB)

Similar as the TLB, the BTLB provides virtual-to-physical address translations. However the *BTLB* maps large address ranges rather that single pages as the *TLB* does. These large address ranges are called *block translations* and therefore stored in the *Block Translation Lookaside Buffer*. These block translations are useful for virtual address ranges that do not get paged in or out.

BTLBs were only implemented on 32-bit PA-RISC processors (PA-7x00), the 64-bit versions instead implement variable page sizes, thus any entry can be of >4k mapping.

2.2.6 Superscalar execution

A *superscalar* processor implementation executes multiple instructions per cycle if dependencies between the instructions permit this.

```
Superscalar: an implementation technique for an instruction
        set architecture that decodes, dispatches, executes
        and returns results from more than one independent
        instruction from an otherwise linear instruction stream
        during each of the processor's basic clock cycle.
                                                ('89, S. McGeady)
```

Every PA-RISC processor from the PA-7100 upwards implements superscalar execution. Instructions proceed together through the execution pipeline which is called *instruction bundling*. The superscalar execution is functionally transparent to the software, the effects of any given instruction are the same whether it was executed as part of a *bundle* or alone. Bundling rules are applied at run-time by the hardware; optimal performance may only be gained by proper ordering of the instructions so the processor can use its full superscalar potential. Additionally there are several kinds of restrictions placed upon the instruction bundling:

- functional unit contention
- data dependency restrictions
- control flow restrictions
- special instruction restrictions

For bundling purposes, all instruction are divided into classes:

class	description
flop	floating point operation
ldst	loads and stores
flex	integer ALU
mm	shifts, extracts, deposits
nul	might nulifiy successor
bv	BV, BE
br	other branches
fsys	FTEST and FP status/exception
sys	system control instructions

PA-7100LC/PA-7300LC superscalar capabilities

These are 2-way superscalar processor implementations with two integer ALUs and one FPU. Notably only one of the two ALUs is capable to handle loads, stores and shifts.

Allowed bundles

first (older) instruction	second (younger) instruction
flop	+ ldst/flex/mm/nul/bv/br
ldst	+ flop/flex/mm/nul/br
flex	+ flop/ldst/flex/mm/nul/br/fsys
mm	+ flop/ldst/flex/fsys
nul	+ flop
sys	never bundled

Besides from these bundles, *ldst* + *ldst* bundles are under certain circumstances also possible. These are then called *double word load/store*.

Data dependencies Several kinds of instructions cannot be bundled together because of inter-instruction data dependencies:

- An instruction that modifies a register will not be bundled with another instruction that takes this register as operand. Exception: a *flop* can be bundled with a FP store of the *flop*'s result register.
- A FP load to one word of a doubleword register will not be bundled with a *flop* that uses the other doubleword of this register.
- A *flop* will not be bundled with a FP load if both instructions have the same target register.
- An instruction that could set the carry/borrow bits will not be bundled with an instruction that uses carry/borrow bits.

Control Flow

- An instruction which is in the delay slot of a branch is never bundled with other instructions.
- An instruction which is at an odd word address and executed as a target of a taken branch is never bundled.
- An instruction which might nullify its successor is never bundled with this successor. Only if the successor is a *flop* instruction this bundle is allowed.

PA-7200 superscalar capabilities

This is a 2-way superscalar processor implementation. It has two integer ALUs and one FPU. Similar to the PA-7100LC, shift-merge and test condition units are not duplicated in the second ALU. To support the superscalar capabilities one additional write port and two additional read ports were added to the general registers (GR*).

Allowed bundles

first (older) instruction	second (younger) instruction
flop	+ ldst/flex/mm/nul/bv/br
ldst	+ flop/flex/mm/nul/br
flex	+ flop/ldst/flex/mm/nul/br/fsys
mm	+ flop/ldst/flex/fsys
nul	+ flop

2.2.7 Multimedia Acceleration eXtensions (MAX-1 and MAX-2)

MAX-1 (32-bit)

The original multimedia extensions were proposed for and later introduced in the PA-7100LC processor. The aim was to enable workstations with this CPU to provide real-time MPEG video decompression and playback at a rate of 30 frames/second without the need for a special DSP (digital signal processing)

chip.

The design process for the PA-7100LC processor (in the early mid-90s) included for the first time multimedia benchmarks while analyzing optimizations for the instruction set design.

The actual implementation was achieved via the introduction of a very small set of SIMD-MIMD *(See Note 1)* instructions to faciliate the application of a small set of instructions on bundled subword data. Since these instructions use the same data paths and execution units within the processor as the 'normal' instructions the term *intrinsic signal processing* (ISP) was coined. By sticking to conventional RISC principles the design team decided against adding complex special-purpose instructions and opted for small, elegant use of the existing processing facilities, which just were modified to understand the new, packed subword data.

In 1994, the extensions made their way to be included in the final PA-7100LC product and as such were the first SIMD *(See Note 1)* instructions found in a general microprocessor. Less than 0.2 percent of the silicon area had to be used for these additions and modifications, while allowing a very significant performance boost in affected applications (for example, the then-highend 735/99 workstation running at 99 MHz with 512KB cache achieves 18.7 fps at MPEG decompression benchmarks, while the new, lower clocked 712 workstation at 60MHz and with 64KB cache achieved 26 fps). New MAX-1 multimedia instructions include: parallel add, parallel subtract, parallel shift left & add (i.e. multiply with integer), parallel shift right & add (i.e. division), parallel average.

Notes

1. Single Instruction Multiple Data, Multiple Instruction Multiple Data (MIMD), see for example the **SIMD Wikipedia article**[18] and **MIMD Wikipedia article**[19]

MAX-2 (64-bit)

With the introduction of the new 64-bit PA-RISC 2.0 architecture in 1996 HP unveiled a new set of multimedia-oriented instructions aimed at using the processor's resources more effectively for sub-word data. The basic components of the contemporary multimedia data were often represented as 8, 12 or 16-bit integers, for example audio sampling and pixel color depth. Doing arithmetic with data of this length would waste an considerable amount of the processor's execution capacities, a simple addition of 16-bit data would only use one quarter of the 64-bit wide integer units datapath. To remedy this situation, MAX allows for packing of these *subword data* into larger words near the processor's natural word width (64-bit on PA-RISC 2.0 processors) and using parallel instructions on them. An example would be four 16-bit additions by the 64-bit adder on four 16-bit packed subwords.

The basic functionality from the earlier 32-bit MAX-1 was taken over and four more instructions added for MAX-2. Additionally, due to the wider integer registers (now 64-bit) more subwords can be packed in one cycle, doubling the effective speed of these multimedia instructions. The MAX-2 multimedia instructions include (new in MAX-2 are in **bold**): parallel add, parallel subtract, parallel shift left & add (i.e. multiply with integer), parallel shift right & add (i.e. division), parallel average, **parallel shift right**, **parallel shift left**, **mix** and **permute**.

[18] http://en.wikipedia.org/wiki/SIMD
[19] http://en.wikipedia.org/wiki/MIMD

MAX-2 debuted 1996 in real silicion on the PA-8000 processor and later featured on all subsequent PA-RISC 2.0 processors (PA-8x00). In contrast to contemporary multimedia extensions, MAX-2 required only very little die space (0.1 percent on the PA-8000).

References

- **Accelerating Multimedia with Enhanced Microprocessor**[20] (PDF, 2.4MB) Discussion of the MAX-1 instructions. Ruby Lee, April 1995, IEEE Micro, Volume 15 Number 2.
- **64-bit and Multimedia Extensions in the PA-RISC 2.0 Architecture**[21] (PDF, 66KB) New features of the 64-bit PA-RISC 2.0 architecture and overview on the MAX introduced with it. Ruby Lee and Jerry Huck, 1996, Hewlett-Packard Company.
- **Subword Parallelism with MAX-2**[22] (PDF, 1.5MB) Discussion of the MAX-2 instructions. Ruby Lee, August 1996, IEEE Micro, Volume 16 Number 4.

[20] http://www.ee.princeton.edu/~rblee/HPpapers/accelMultimediawEnhancedMicroproc.pdf
[21] http://ftp.parisc-linux.org/docs/whitepapers/pa2c96.pdf
[22] http://www.eecs.harvard.edu/~dbrooks/cs146/lee96subword.pdf

2.3 PA-RISC Chipsets

2.3.1 Overview

This page discussed several I/O-chipsets used throughout the PA-RISC line of computers. A good deal of information exists due to the availabilty of technical documentation from HP for open-source OS projects. Information on more chipsets will be added.

2.3.2 ASP

Used in

- 705 and 710
- 715/{33,50,75}
- 725/{50,75}
- 720, 730, 750
- 735 and 755 (*ASP2*)
- 742i/50
- 745i/{50,100}
- 747i/{50,100}

ASP is the the chipset used in all older PA-RISC workstations, still being a 'classical' chip**set**, it includes several different chips to provide the I/O-subsystem. It includes several modules from 3rd party vendors to complete the system. The ASP**2** chipset, used in the 735 and 755 workstations, offers some small feature improvements (faster SCSI and addditional FDDI networking).

Features

- *Viper* memory controller
- NCR 53C700 8-bit Narrow single-ended SCSI-2
- ASP2: NCR 53C720 16-bit Fast-Wide *differential* SCSI-2
- Intel 82596DX 10Mb Ethernet controller
- Intel 82501AD Ethernet transceiver, media auto-selection
- ASP2: AMD Formac Plus Am79C830 FDDI controller (*ASP2*)
- ASP2: Stereo/CD quality audio
- WD 16C552 parallel
- NS 16550A compatible serial
- 512KB EPROM - the Boot ROM
- 8KB EEPROM for storing system configuration status etc.
- Intel 8042 microprocessor controlling:

  - battery backed RTC
  - system & user timers
  - audio generator
  - HP-HIL interface
  - frontpanel system status LEDs

References

- **Hardball ERS - 735/755 (ASP2)**[23] (PDF, 4.2MB)

2.3.3 Astro

Used in

- A400 (rp2400, rp2430), A500 (rp2450, rp2470)
- B1000, B2000, B2600
- C3000, C3600, C3700
- J5000, J5600, J6000, J6700, J7000, J7600
- L1000 (rp5400), L2000 (rp5450)

Newer workstations use the Astro chip for memory and I/O management. It includes most of the functions on a single die, requiring only few additional peripheral ASICs to interface and drive the specific buses.

Features

- peak memory bandwidth of 2GB/s
- support for 125MHz SDRAM
- maximum supported memory of 40GB
- PCI 2.1 compliant
- 8 I/O *ropes* for high flexibility
- aggregate bandwidth of more than 1GB/s
- 16-entry fully associative I/O TLB
- 16-entry fully associative coherent I/O buffer cache

References

- **Astro ERS Overview**[24] (PS, 0.1MB)
- **Astro ERS Error Handling**[25] (PS, 1.5MB)

[23] http://ftp.parisc-linux.org/docs/chips/hardball_ers.pdf
[24] http://ftp.parisc-linux.org/docs/chips/astro_intro.ps
[25] http://ftp.parisc-linux.org/docs/chips/astro_errors.ps

- **Astro ERS R2I Operations**[26] (PS, 2.3MB)
- **Astro ERS Register Map**[27] (PS, 0.3MB)
- **Astro Runway Interface**[28] (PS, 2.0MB)
- **Astro Memory Map**[29] (PS, 0.1MB)

2.3.4 Dino/Cujo

1FC3-0004

Used in

- A180, A180C
- C132L, C160L, C160, C180, C200, C240, C360
- J2240
- RDI PrecisionBook 132, 160, 180

Dino is the GSC-to-PCI bridge found in most older PCI-based PA-RISC workstations. The GSC and PCI bus do not need to be synchronized, simplifying the system design. each bus. Dino also implements a small set of I/O-functions.

Cujo is a Dino bridge with an 64-bit datapath.

Features

- Implements GSC+ features
- Mapping register with 8MB resolution
- Integrated PCI arbitration
- Integrated interrupt register
- Supports >40MHz GSC operation
- Supports >33MHz PCI operation
- two PS/2 interfaces
- RS-232 port
- Supports both 3.3V and 5.0V PCI operation
- 208-pin PQFP package

References

- **DINO ERS**[30] (PS, 5.8MB)

[26] http://ftp.parisc-linux.org/docs/chips/astro_ioc.ps
[27] http://ftp.parisc-linux.org/docs/chips/astro_regmap.ps
[28] http://ftp.parisc-linux.org/docs/chips/astro_runway.ps
[29] http://ftp.parisc-linux.org/docs/chips/astro_sysmap.ps
[30] http://ftp.parisc-linux.org/docs/chips/dino_ers.ps

2.3.5 Elroy

Used in

- A400 (rp2400, rp2430), A500 (rp2450, rp2470)
- B1000, B2000, B2600
- C3000, C3600, C3700
- J5000, J5600, J6000, J6700, J7000, J7600
- L1000 (rp5400), L2000 (rp5450)
- N4000
- Superdome

Elroy is the chip used to interface PCI to the system-bus in the various newer PA-RISC systems. Several Elroy ASICs can be and are used in these systems to attach several PCI buses.

Features

- peak bandwidth of up to 500MB/s
- support for *Turbo-Channel* and *Twin Turbo-Channel* (not related to the DEC TurboChannel)
- support for PCI 2.1, 1X, 2X and 4X protocol
- PCI-width of either 32 or 64 bit
- PCI-clock of 30-66MHz

References

- **Elroy ERS**[31] (PS, 4.7MB)

2.3.6 LASI

1FT1-0002, 1FU2-0002

Used in

- 712/{60,80,100}
- 715/{64,80,100}
- 725/100
- 743i/{64,100}
- 744/{132L,165}
- 748i/{64,100,132,165L}
- A180, A180C

[31] http://ftp.parisc-linux.org/docs/chips/elroy_ers.ps

- B132L, B132L+, B160L, B180L+
- C100, C110, C132L, C160L, C160, C180, C200, C240, C360
- D-Class
- E25, E35, E45, E55
- J200, J210, J210XC, J280, J282. J2240
- K-Class
- RDI PrecisionBook 132, 160, 180
- R380, R390
- SAIC Galaxy 1100

Designed for and firstly used in the 712 series workstations the LASI I/O chip was similarly designed for cost-reduction. One of the major objectives of the 712 I/O subsystem was to provide similar or equal functionality and performance like other 700 series systems (e.g. 720, 730, 715 Scorpio) at a significantly reduced manufacturing cost. The design team finally concluded that integrating major parts of the I/O subsystem into one large VLSI chip would reduce the fabrication cost significantly, as required. The majority of circuitry in LASI is consumed by the two most important parts: LAN and SCSI (therefore **LAN SCSI**). Both of these designs were purchased from third party companies (NCR and Intel) and integrated as so-called mega-cells in the VLSI chip. The other I/O functions originate from HP internal standard cell designs, some of whom were leveraged from previous HP ASIC designs and some designed specifically for LASI.

Features

- LAN - Intel i82C596CA 10Mb Ethernet controller
- SCSI - NCR 53C710 Fast-Narrow SE SCSI-2 controller
- Serial - NS16550A compatible RS232
- Parallel - WD16C522 compatible
- Audio - *Harmony* CD-quality 16-bit sound
- Telephony - optional expansion, support for two lines
- Human Interface - support for two PS/2 style keyboard and mouse devices
- FDD and boot ROM - external 8-bit bus to connect flash EPROMs and a FDD-controller (WD37C65C)
- Interface to GSC bus
- Bus arbitration
- Interrupt controller
- Real-Time clock (*RTC*)
- PLL generator for the whole I/O subsystem

Besides this chip only very few parts are needed to build a complete system: CPU, cache, RAM and a graphics adaptor. It is furthermore possible to use up to four LASI chip on a single GSC bus. The LASI chip was designed in a 0.8u CMOS process and is 13.2 x 12.0 mm$\hat{2}$ in size. It contains 520,000 FETs and is packaged in a 240-pin MQUAD package. It consumes about 3W when operating an 40MHz.

References

- **LASI ERS**[32] (PS, 4.3MB)
- **Design of the Model 712's I/O subsystem (LASI)**[33] (PDF, HP Journal 4/95)

[32] http://ftp.parisc-linux.org/docs/chips/lasi_ers.ps
[33] http://www.hpl.hp.com/hpjournal/95apr/apr95a4.pdf

2.4 PA-RISC Buses

2.4.1 EISA

The *Extended ISA* bus was meant to replace the older ISA bus and therefore it inherited several details from it. An EISA bus is available in several series 700 systems, either onboard or by a seperate adaptor.

- 32-bit data path width
- 33MB/s maximum transfer rate
- 5V signalling voltage
- EISA slots also accept 8/16-bit ISA cards
- 200-pin(50x2x2) edge male card connector
- Bulkhead is left of the card

2.4.2 GSC/HSC

The *General System Connect* bus is the primary I/O bus on most of the 700s workstations. It connects most of the I/O devices to the system bus. Some CPUs directly attach to the GSC bus (PA-7100LC and PA-7300LC). There appeared several different variants of GSC cards:

Different speeds

- standard
- +
- 2x

Different formfactors (FFs)

- EISA
- GIO
- HSC
- GSC-M (GSC-mezzanine)

- 32-bit data path width
- Multiplexed address and data
- 160MB/s (*standard*) or 250MB/s (*2x*) maximum transfer rate
- GSC-M: 142MB/s maximum transfer rate
- 5V signalling voltage
- 100-pin (50x2) female EBBL card connector (*EISA FF*)
- 100-pin (50x2) male pin+socket with groundplane (*HSC FF*)
- 80-pin (40x2) female EBBL card connector (*GIO FF*)
- 100-pin (50x2) male pin+socket with groundplane (*GSC-M*)

- Bulkhead is left of the card (*EISA FF*)
- Bulkhead is right of the card (*GIO FF*)
- Bulkhead is above the card (*HSC FF*)
- Bulkhead is below the card (*GSC-M*)

2.4.3 HP-PB

The *HP-Precision Bus* is the I/O-bus in most of the older Series 800 servers. There are basically two formfactors: *single* and *double* (like 2U VME).

- 32-bit data path width
- 23MB/s maximum transfer rate
- 5V signalling voltage
- 96-pin (32x3) female pin+socket card connector

2.4.4 PCI

With PCI, HP tried to change its workstation designs to faciliate a standard expansion/device bus, making it possible to use more cheaper, off-the-shelf products such as I/O-chips without the need to building GSC/SGC interfaces for these.

Moreover, there was a great deal more PCI expansion cards manufactured than e.g. GSC or SGC ones, driving down the design costs of expansion cards. Some of HP's PCI expansion cards are relabeled 3rd party products or OEM designs which only needed an HP-compatible firmware and the belonging HP-UX driver.

The latter fact is the limiting factor in using 3rd party PCI expansion cards in HP 9000 boxen running HP-UX. Mostly, HP supplied only drivers for their own HP-branded products, using e.g. Adaptec SCSI cards or 3Com NICs is in most cases impossible since no HP-UX drivers exist for them.

When using an Open Source OS such as e.g. Linux or OpenBSD it is more likely that a driver for the specific expansion card already exists and was/can be ported to the PA-RISC port.

PCI	Clock	Width	max data rate	Signalling
PCI-32/33	33MHz	32-bit	132MB	3.3V/5V
PCI-32/66	66MHz	32-bit	264MB	3.3V
PCI-64/33	33MHz	64-bit	264MB	3.3V/5V
PCI-64/66	66MHz	64-bit	528MB	3.3V
PCI-64/100	100MHz	64-bit	762MB	3.3V
PCI-X	133MHz	64-bit	1026MB	?

Any PCI-card should run in any PCI-slot, given that the voltage (3.3V/5V) is the same. Slower cards in faster slots will reduce the overall PCI bandwidth of that particular bus.

2.4.5 Runway

Runway is the system bus newer PA-RISC CPUs (PA-7200 and PA-8000 upwards) connect to. It is a synchronous, split-transaction bus.

- 1-4 CPU glueless SMP
- 64-bit multiplexed address/data
- 20 bus protocol signals
- supports cache coherency
- two frequency options (1/1 and 2/3 of CPU clock)
- parity protection on address/data and control signal
- each attached device contains its own arbitrator logic
- split transactions, up to six transactions can be pending at once
- snooping cache coherency protocol
- 768MB/s sustainable throughput, peak 960MB/s
- on PA-8500, the bus operates in a DDR *(double data rate)* mode, resulting in a peak bandwidth of about 2GB/s

References:

- **Runway Bus introduction**[34] (PDF, HP Journal 2/96)

2.4.6 SGC

The *System Graphics Connect* bus is basically the mainbus of the older series 700 computers. Thus the SGC-expansion cards directly attach to the mainbus in these systems. There are also two different form-factors: *EISA* and *DIO*.

- 32-bit data path width
- 100MB/s maximum transfer rate
- 5V signalling voltage
- 176-pin (44x4) female pin&socket card connector (*DIO-II FF*)
- 160-pin (40x4) male EBBL card connector (*EISA FF*)
- Bulkhead is above the card (*DIO-II FF*)
- Bulkhead is right of the card (*EISA FF*)

[34] http://www.hpl.hp.com/hpjournal/96feb/feb96a2.pdf

2.5 PA-RISC Expansion Cards

2.5.1 Cards

Here is an incomplete list of expansion cards for PA-RISC computers sold (mostly) by HP and (hopefully) supported by HP-UX.

2.5.2 EISA/ISA

- A2544A - ATR/9000 Link
- A2545A - ATR/9000 & EISA slot (*only for 720*)
- A2679A - Fast SCSI-2 host adaptor *(See Note 1)*
- A3402A - 10/100VG LAN interface
- A3658A - 100BaseT Ethernet interface
- A3659A - FDDI interface
- A4031A - Fiberchannel interface 266Mb
- A4308A/A4308B - 100BaseT Ethernet interface
- B5502AA - FDDI interface
- E2070A/B/C - HP-IB interface, normal speed (*ISA*)
- E2071A/B/C/I - HP-IB interface, high speed
- E2074A/B - GPIO interface
- J2104A - ISDN BRI (*ISA)*)
- J2109A - ISDN BRI (for the US) (*ISA*)
- J2159A - X.25 interface
- J2165A - IEEE 802.5 token ring interface
- J2220B - Programmable Serial Interface
- J2226A - SNAplus link
- J2482A - 8-port RS232C multiplexer
- J2483A - 64-port RS232C multiplexer
- J2645AA - 10/100VG LAN interface (no Ethernet!)
- J2794A - X.25 interface
- J2802A - ATM interface, OC3/155Mb (*only 700 series*)
- J2802B - ATM interface, OC3/STS-3c 155Mb (*only 700 series*)
- J2815A - dual port Programmable Serial Interface
- 25525A/25525B - narrow (8-bit) HVD SCSI-2 interface
- 25560A - HP-IB interface, high speed

- 25567-60003 - EISA LAN card
- more ...

Other Vendors

- Interphase WA-C321T-UX - FDDI SAS interface
- Interphase WA-C323T-UX - CDDI SAS interface
- Interphase WA-C326T-UX - FDDI DAS interface
- Interphase WA-C328T-UX - CDDI DAS interface
- Interphase 4811 - FDDI single MIC, single/dual UTP, single/dual STP
- Interphase 4824 - 100BaseT/10BaseT Ethernet interface **ftp://ftp.iphase.com/pub/ethernet/eisa/**[35]
- MDL Corp. FAWS - wide single-ended SCSI-2 interface
- MDL Corp. FAW - wide differential SCSI-2 interface
- Parallax XVideo 700 - Video export/import
- Qualix IW-h100 - Phobos 10BaseT interface
- SBE WSU 432S - wide single-ended SCSI-2 interface
- SBE WSU 432D - wide differential SCSI-2 interface
- FE Phobos H100 Fast EISA Ethernet (HP-UX driver mirror: **http://ftp.halcyon.com/pub/users/mdlcorp/100ba**
- 3Com 3c597-TX EISA Fast Ethernet, should work with the above Phobos driver

Notes

1. Unsupported on J-Class. B and C-Class require card revision -0003 or later.

2.5.3 GSC/HSC

The default formfactor of GSC cards is sized similarly to an standard EISA card, so it is called *EISA formfactor*; there was also the *HSC* (about 3x5 inches) and *GSC-M* form-factor. Some GSC>+ cards are also called HSC, but in fact are in the EISA formfactor

EISA formfactor

- A2874-66005 - Fast-Wide high-voltage differential (HVD) SCSI-2 interface
- A4107A - wide SCSI-2 interface
- A3723A - FDDI interface
- A4070A/A4070B - HCRX-8 graphics
- A4071A/A4071B - HCRX-24 graphics

[35] ftp://ftp.iphase.com/pub/ethernet/eisa/
[36] http://ftp.halcyon.com/pub/users/mdlcorp/100baseT/

- A4072A - 3D accelerator for any HCRX graphics
- A4073A/A4073B - CRX-48Z GSC interface (for CRX-48Z graphics processor)
- A4074A - CRX-48Z graphics processor
- A4077A/A4077B (A4081-66009) - CR 2D 8-bit color graphics
- A4078A - Dual CR 2D graphics
- A4079A/A4079B - HCRX-8Z graphics (*in fact is A4070B + A4072A*)
- A4179A - HCRX-24Z graphics (*in fact is A4071B + A4072A*)
- A4211A - Visualize-48 graphics
- A4242B - Z-Buffer + accelerator for HCRX graphics
- A4244A - Visualize-48 graphics
- A4245A - texture memory for the above
- A4246A - Visualize-48XP graphics, EVC connector
- A4247A - texture memory for the above
- A4247A - video export daughter card for HCRX graphics
- A4253-69001 - Freedom Interface graphics, 13W3 connector
- A4253A - Freedom S3150 graphics accelerator
- A4254A - Freedom S3250 graphics accelerator
- A4255A - Freedom S3400 graphics accelerator
- A4333A - Visualize-IVX graphics, daughter card to HCRX graphics
- A4441A - Visualize-8 graphics (*in fact is A4070B + A4242A*)
- A4442A - Visualize-24 graphics (*in fact is A4071B + A4242A*)
- A4443A - upgrade HCRX-{8,24}Z to Visualize-{8,24}
- A4450A - Visualize-EG graphics, EVC connector
- A4451A - Dual Visualize-EG graphics, EVC connector
- A4452A - 2MB add-on memory for A4450A & A4451A
- A4925A (A4925-60001) - 1000BaseSX fibre Gigabit-Ethernet
- A4926A - 1000BaseSX Gigabit-Ethernet interface
- J2498A - ATM interface, 155Mb
- J2499A - ATM interface, OC3c 155Mb
- J3515A - 100BaseT/10BaseT/AUI Ethernet interface
- J3516A - 100BaseT/10BaseT dual port Ethernet interface
- more ...

HSC formfactor

- A2969A (A2926-60001) - Fast-Wide Differential (HVD) SCSI Adapter.
- A2999A - Color graphics, Dsub15 connector
- A3519A - Visualize-EG graphics, EVC connector
- A4455A - Visualize-48XP graphics, EVC connector
- J2499A (J2499-60011) - ATM interface, OC3c 155Mb
- J3514A (J3514-60001) - Dual 10/100Mbit Ethernet interface
- more ...

GSC-mezzanine (GSC-M)

- A4267A - 8-plane graphics
- A4268A - Fast-Wide *high-voltage differential* (HVD) SCSI
- A4315A - HCRX-8 graphics
- A4316A - HCRX-24 graphics
- J3420A - ATM card

2.5.4 SGC

There are two types of SGC expansion cards: the bigger cards, called *DIO-II formfactor* and the EISA-like (*EISA formfactor*) cards.

DIO-II formfactor

- A1439A - CRX-24 graphics
- A1454A - CRX-24Z, Z-buffer daughter board for the above card
- A1471A - Personal VRX graphics, RGB BNC
- A1472A - Turbo VRX graphics, RGB BNC
- A1659A - CRX graphics
- A1924A - GRX graphics
- A1986A - EISA slot for model 720
- A2091A - CRX-48Z graphics processor, (*external break-out box*)
- A2091A-66580 - CRX-48Z SGC interface (for the above)
- A2262A - Dual CRX graphics
- A2269A - Non-CRX to Dual-CRX graphics/Dual-CRX to Quad-CRX graphics upgrade
- A2270A - CRX-24 to Dual CRX-24 graphics upgrade
- A2271A - CRX to CRX-24 graphics upgrade

- A2288-66003 - Audio-adapter board with room for optional FDDI slider
- A2666A - CRX-24Z to CRX-48Z graphics upgrade
- A2667A - PVRX to CRX-48Z graphics upgrade
- 98705P - P-VRX P3 graphics, RGB BNC
- 98768A - CRX graphics upgrade
- more ...

EISA formfactor

- A2673A - CRX-24 graphics interface
- A2674A - CRX-24Z, Z-Buffer daughter board for the above card
- A2675A - CRX-48Z graphics interface processor, (*external break-out box*) with A2675-66581 - CRX-48Z SGC interface
- A2804A - EISA slot for model 715
- more ...

2.5.5 GIO/TSIO

GIO is the special formfactor of GSC expansion cards for 712 systems.

- A2878A - second video
- A4011A - 8025 Token Ring interface
- A4011B - 8025 Token Ring interface
- A4013A - second serial port
- A4014A - second LAN (AUI+TP) and serial port. Pinout for the AUI/RS232 Y-cable
- A4015A - second serial & X25 link (DB9M RS232C connectors)
- A4217A - second LAN (AUI+TP) & second VGA
- TAMS 50488 - HP-IB interface

TSIO is another special formfactor GSC card for the *Teleshare* expansion slot found in 712s.

- A4012A - Teleshare POTS interface with (2) RJ11C

2.5.6 HP-PB

There are two types of HP-PB expansion cards: single and double height.

- 28696-60001 - 16-bit differential (HVD) SCSI, double-height
- 28670-60101 - DAS FDDI with MIC connector, double-height
- 28640-60001 - 10Mbit Ethernet AUI/BNC, single.height

- A3495A (A3495A-60001, A3495A-60301) 10/100Mbit Ethernet TP, single-height
- J2157A - FDDI
- J2146A - 10Mbit Ethernet, single-height

2.6 HP 9000 Memory Modules

2.6.1 Overview

There are basically three types of memory PA-RISC workstations and servers use:

1. Proprietary boards. Used by the first 700s workstations and by the older servers. Boards are interchangable, i.e. all these machines can use any of these boards.
2. Old 72-pin ECC SIMMs. Used almost throughout the whole line of numbered 700s workstations and several servers. Should also be interchangeable, some incompatibilities could occur though.
3. Newer 72-pin ECC SIMMs. Used by the newer, lettered workstations. Basically same as the above but with shorter cycle-times (60, 50ns). Interchangeable but some machines (with PA-8x00 CPU) need the faster 50ns modules.

On a side note relating the 72-pin SIMMs: *these are* **not** *compatible with other popular workstations as for example SGI, DEC Alpha or even PCs.* These HP ECC SIMMs only work in HP 9000 PA-RISC systems (and some Laserjets) and, at least to my knowledge, not in any other computer. Alas, 72-pin (36-bit parity) SIMMs that may work in PCs or in one of the above mentioned workstations will not work in HP 9000 systems.

2.6.2 Proprietary boards

Used in:

- 720, 730, 750
- 735 & 755
- Nova servers

Although all of these boards would fit electronically some are a bit too tall to fit in the desktop 700s, namely 720, 730 and 735. So take care and look if the modules will fit physically in your system.

Original HP part numbers:

- A2521A - 720 CPU and 96MB
- A2522A - 720 CPU and 128MB
- A2531A - 730 CPU and 96MB
- A2532A - 730 CPU and 128MB
- A2521A - 720 CPU and 96MB
- A2668A - 720 32MB upgrade
- A2562A - 720 64MB upgrade
- A2669A - 730 32MB upgrade
- A2567A - 730 64MB upgrade

- A2533A - 750 256MB upgrade
- A2534A - 750 384MB upgrade
- A1978A - (2) 4MB modules
- A1979A - (2) 8MB modules
- A2512A - (2) 16MB modules
- A2513A - (2) 32MB modules
- A2518A - (2) 64MB modules

2.6.3 Old 72-pin ECC SIMMs

Used in:

- 712/{60,80,100}
- 715/{33,50,75}
- 715/{64,80,100}
- 725/{50,75,100}
- 745i/{50,100}
- 747i/{50,100}
- E25, E35, E45, E55

Original HP part numbers:

- A2577A - (2) 4MB 72-pin SIMMs
- A2578A - (2) 8MB 72-pin SIMMs
- A2829A - (2) 16MB 72-pin SIMMs
- A2827A - (2) 32MB 72-pin SIMMs
- A2815A - (2) 4MB 72-pin SIMMs
- A2816A - (2) 8MB 72-pin SIMMs
- A2829A - (2) 16MB 72-pin SIMMs
- A2827A - (2) 32MB 72-pin SIMMs
- A2875A - (2) 64MB 72-pin SIMMs

705 and **710** use different, even older 72-pin SIMMs which mostly don't work in any other HP 9000. (Modules from e.g. 712 or 715 won't work in the 705/710 neither):

- A2216A - (2) 4MB SIMMs
- A2217A - (2) 8MB SIMMs
- A2218A - (2) 16MB SIMMs

2.6.4 Newer 72-pin ECC SIMMs

Used in:

- A180, A180C
- B132L, B132L+, B160L, B180L+
- C100, C110, C132L, C160L, C160, C180, C200, C240
- J200, J210, J210XC, J280, J282
- D-Class

Original HP part numbers:

- A3026A - (2) 16MB 60ns ECC SIMMs
- A4207A - (2) 16MB 60ns ECC FPM SIMMs
- A4209A - (2) 32MB 60ns ECC FPM SIMMs
- A4515A - (2) 32MB *50ns* ECC EDO SIMMs
- A3027A - (2) 64MB 60ns ECC SIMMs
- A4208A - (2) 64MB 60ns ECC FPM SIMMs
- A3408A - (2) 64MB 60ns ECC DIMMs
- A4516A - (2) 64MB *50ns* ECC EDO SIMMs
- A4177A - (2) 128MB *50ns* ECC EDO SIMMs
- A4517A - (2) 128MB *50ns* ECC EDO SIMMs
- A3564A - (2) 128MB 60ns ECC EDO SIMMs
- A3717A - (2) 256MB 60ns ECC EDO SIMMs

2.6.5 743i ECC mezzanine cards

Used in:

- 743i/{64,100}
- 748i/{64,100}

The VME SBCs use special ECC mezzanine cards, up to four board can be used in on of these systems.

Original HP part numbers:

- A4263A - 8MB RAM card
- A4264A - 16MB RAM card
- A4265A - 32MB RAM card
- A4266A - 64MB RAM card

2.6.6 744 ECC mezzanine cards

Used in:

- 744/{132L,165L}
- 745/{132L,165L}
- 748/{132L,165L}

The VME SBCs use special ECC mezzanine cards, up to four board can be used in one of these systems. They use faster versions of the above mentioned *743i ECC mezzanine cards*.

Original HP part numbers:

- A4501A - 16MB RAM card (only supported by HP-RT OS)
- A4502A - 32MB RAM card
- A4503A - 64MB RAM card
- A4449A - 128MB RAM card
- A6005A - 256MB RAM card

2.7 PA-RISC Boot-ROM

2.7.1 Overview

Every PA-RISC computer includes a firmware, which is called *PDC*. This implements all the processor-dependent functionality, similar to the BIOS found in x86 systems. After power-up of the system, the PDC initializes the CPU and performs some self-tests on the whole system and the subsystems. If it detects any errors, it displays an error-code on the front-LEDs. Upon successful completion it loads the ISL *(Initial System Loader)* and transfers control to it, so the ISL can load the OS from your preferred media.

The PDC must know the device on which the ISL can be found on though. To do so the PDC looks up the *Primary Boot Path* which is stored in the "Stable Storage". If the processor is reset after self-test and initialization the PDC tries to determine what device you are using as system-console. It first reads the *Console Path* from the "Stable Storage" and tries to initialize this device; if that fails (e.g. PATH 'console' is set to "graphics" and you've removed the framebuffer) the PDC tries to find a valid device. The algorithms used to find this device vary throughout the whole series 700.

If the `AUTO` flags are set in the PDC, it waits for 10 seconds during which you can interrupt the autoboot/search process with `<ESC>` and get to the boot administration prompt. If you don't interrupt this process, the PDC searches bootable devices for an *IPL* and boots these after announcing it.

If boot is interrupted, a plain menu is displayed, where you can:

- choose the device you want to boot from
- start a search for bootable devices containing an IPL
- enter the boot administration prompt

2.7.2 Boot administration menu on workstations

If you interrupted the autoboot process and chose `a` you get to this menu. Here you can alter the auto* flags, the boot/console/etc-paths, monitor types and much more. You have the following commands available (differ from machine to machine):

command	parameters	description
`AUTO`		displays the current state of the AUTOBOOT & AUTOSEARCH flags.
`AUTOSEARCH`		toggles whether or not the PDC automatically searches for bootable devices.
`AUTOBOOT`		toggles whether or not the PDC automagically boots the device described in either *primary* or *alternate* `PATHs`.
`BOOT`	`[device [isl]]`	boots from specified `device` or one of `pri` or `alt`.
`DATE`		sets or reads the RTC.
`EXIT`		Leave the PDC.
`FASTSIZE`		sets or reads the value of the FASTSIZE memory parameter.

HELP	[item]	shows general/item-specific information.
INFO		gives info about the hardware, e.g. CPU/IO/SCSI-frequency, which LAN-port is used, revision of the various chips and the PDC.
LAN_ADDR		shows the MAC-address of the Ethernet controller.
OS		pretty useless nowadays
PATH	[path_type [device]]	displays or sets either path_type or all paths in the Stable Storage. path_type can be: primary, alternate, console and keyboard.
PIM_INFO		displays internal memory of the CPU, e.g. registers, stack.
RESET		resets the system.
SEARCH	[device [ipl]]	search either all device interfaces or just specified device interface for bootable media or IPL.
SECURE		displays or sets the secure boot mode flag. If ON you can't interact with the system in the first 10s before device selection. Pretty pointless.
SHOW		shows the results of the previous SEARCH.

Devices

The following devices may exist on a 700s workstation and can be referenced in the PDC:

- `eisa.*`: cards in the EISA-slot(s)
- `lan.*`: one of the network adaptors
- `graphics[_1,_2]`: one of the video adaptors
- `hil`: HIL-input devices
- `parallel`: the parallel printer port
- `rs232_a.*`: the first serial port
- `rs232_b.*`: the second serial port

2.7.3 Examples

Some easy examples on using the PDC:

1. If you want to see the current value of the console PATH, e.g. howto control the input, type:

   ```
   BOOT_ADMIN> PATH console
   ```

2. If you want to change this variable to the first serial port, type:

   ```
   BOOT_ADMIN> PATH console rs232_a
   ```

3. If you want to the PDC to search for bootable media, type:

   ```
   BOOT_ADMIN> SEARCH ipl
   ```

4. If you want to search only the local SCSI bus, type:

   ```
   BOOT_ADMIN> SEARCH scsi ipl
   ```

5. If you want to search for RBOOTD or BOOTP servers, type:

   ```
   BOOT_ADMIN> SEARCH lan
   ```

6. If you want to boot from the SCSI device at ID 6, type:

   ```
   BOOT_ADMIN> BOOT scsi.6 isl
   ```

7. If you want to boot HP-UX 10.20 in *single-user* mode to e.g. repair the system, type:

   ```
   BOOT_ADMIN> BOOT scsi.6 isl ISL> hpux -is
   ```

2.8 PA-RISC LED codes

2.8.1 Overview

Most PA-RISC computers have some LEDs on the system's front-panel. If an error occurs during the power-up diagnostic tests, the PDC uses the front panel LEDs to display a code for the failing component(s).

705/710, 715/{33,50,75}, 715/{64,80,100} and **725** have 9 LEDs on the front-panel:

A = Amber, G = Green.

8	7	6	5	4	3	2	1	0
A	A	A	A	A	A	A	A	G

0 is the Power LED, it indicates that the system is powered up. 4 is the *heartbeat*; if the system is running, it flashes periodically to indicate that the system is still alive.

Similarily, 720/730/750 and 735/755 have 10 LEDs (Illustration):

9	8	7	6	5	4	3	2	1	0
G	A	A	A	A	A	A	A	A	G

The only difference is LED no. 9, the "Service LED", indicating whether the machine was to boot in "Service mode". On 755 these LEDs are arrangend from top to bottom, starting with LED 0, the Power LED.

Newer machines like e.g. B-Class or C-Class only have 5 LEDs: one Power LED and four System LEDs. (Illustration):

2.8.2 712

The 712 only has two error-messages that are displayed on the LED above the power button:

1. a 3/4-second flash pattern: CPU board is defective
2. a "three quick flashes, pause, three quick flashes"-pattern: graphics hardware problem

2.8.3 715 (Scorpio)

Taken from the *Model 715 Owner's Guide*, these codes apply to 715/{33,50,75} they should be applicable to other 700.

means LED is on or flashing, **/** means LED is either on or off

8 7 6 5 4 3 2 1	**Error Message**	**Solution**
_ _ _ # / / / /	CPU/FPU error	probably replace mainboard/CPU
_ _ # _ / / / /	"	"
_ _ # # / / / /	CPU/Motherboard error	"
_ # _ _ / / / /	CPU/FPU error	"
_ # _ _ # _ _ #	FPU-test failure	If it doesn't disappear, power down the system & reboot. If unsuccessful, replace cpu-card
_ # _ _ # _ # _	"	"

_ # _ _ # _ # /	"	"
_ # _ # _ _ _ #	EISA-interface error	Remove all EISA-cards, remove EISA-backplane etc. Clean, and reinstall in the system. If error still appears one of former is broken and to be removed.
_ # _ # _ _ # _	"	"
_ # _ # _ _ # #	"	"
_ # _ # _ # _ _	"	"
_ # _ # _ # _ #	"	"
_ # _ # # # # #	PDC ROM checksum error	?
_ # # _ _ # # #	Memory pair 0, Slot B error	Pull out module in question, clean, reseat. If error still appears memory-module is broken.
_ # # _ _ # # _	Memory pair 0, Slot A error	"
_ # # _ _ # _ #	Memory pair 1, Slot B error	"
_ # # _ _ # _ _	Memory pair 1, Slot A error	"
_ # # _ _ _ # #	Memory pair 2, Slot B error	"
_ # # _ _ _ # _	Memory pair 2, Slot A error	"
_ # # _ _ _ _ #	Memory pair 3, Slot B error	"
_ # # _ _ _ _ _	Memory pair 3, Slot A error	"
_ # # # # # _ #	No memory found	Better start machine with some memore
# _ _ _ _ _ _ _	Unknown I/O device	Pull out all unneccessary devices and reboot
# _ _ _ _ _ _ #	Error while trying to boot from SCSI device	Check SCSI-bus for cabling and termination errors, check drives
_ # _ _ _ _ _ #	Error while trying to boot from LAN	Check cabling
# _ _ _ _ _ _ #	Error trying to access Console Keyboard	Check HIL-cabling polarity, try different keyboard
# _ _ _ _ # _ _	Error while trying to access Console Device on COM1	Check cable and terminal [settings]
# _ _ _ _ # _ #	Error while trying to access Console Device on COM2	Check cable and terminal [settings]
# _ _ _ _ # # _	Error while trying to access Parallel port	Bad luck
# _ _ _ _ # # #	Error on SGC Slot 1 (built-in Gfx)	Remove card, clean, reseat, maybe try another one
# _ _ _ # _ _ #	Unable to initialize EISA slot	Remove EISA card, backplane, clean both, reseat
# _ # # _ _ _ #	Error reading from Stable Storage/EEPROM	Switch off, pull cord. Re-plug, and restart
# _ # # _ _ # _	Unexepected interrupt during PDC execution	Same as above
# _ # # _ _ # #	No working console found	Attach one
# _ # # _ # _ _	HPMC handling initiated	?
# _ # # _ # _ #	HPMC due to cache error	Switch off and reboot, if problem persists the cache is probably defect. Get new CPU or motherboard
# _ # # _ # # _	HPMC due to memory error.	Switch off and reboot. Reseat/replace memory boards.
# _ # # _ # # #	HPMC due to bus error.	Switch off and reboot, if problem persists a core component is probably defect. Get new CPU or motherboard
# _ # # # _ _ _	Nested HPMC occured.	Switch off and reboot. (very bad)
# _ # # # _ _ #	Error while writing to EEPROM.	?

# _ # # # _ # _	Unable to determine valid Processor Speed.	?
# _ # # # _ # #	ROM Checksum error.	?
# _ # # # # _ #	Illegal Processor Speed/Clock Ratio sensing.	?
# _ # # # # # #	Bad Memory Hardware.	?

2.8.4 715 (Mirage)

Taken from the Model 715 Owner's Guide, these codes apply to 715/{64,80,100} they should be applicable to other 700s.

means LED is on or flashing, **/** means LED is either on or off.

8	7	6	5	4	3	2	1	Error Message	Solution
	#						#	CPU Error	?
		#				#	#	Fatal Error	?
		#					#	RAM Test Error	?
	#					#		Cache Error	?
	#				#			FP Coprocessor Error	?
		#			#			Fatal Coprocessor Error	?
	#			#				I/O Device Error	?
	#					#	#	ROM Checksum Error	?
		#		#	#			HPMC Error	Switch Machine off, reboot. Could indicate failure of a core component
		#				#		HPMC due to Cache Error	Switch Machine off, reboot. Indicates drastic failure in cache subsystem. If possible, replace cache/CPU module
		#			#		#	HPMC due to Bus Error	Switch Machine off, reboot.
		#			#	#	#	HPMC due to Memory Error	Switch Machine off, take the RAM out. Figure out, which module is broken.
	#	#		#			#	Console Initialization Error	Look if keyboard/serial console cable is attached properly.
		#		#		#		No working console found.	"
	#	#		#		#		No bootable device found.	Install one, check PATHs
	#	#			#	#		InitializationError	?

2.8.5 720/730/750 (Snakes)

Taken from the Owner's Guide. Illustration of the LED panel.

means LED is on or flashing, **/** means LED is either on or off

8	7	6	5	4	3	2	1	Error Message	Solution
			#	/	/	/	/	CPU Error	Replace processor board
		#		/	/	/	/	CPU Error	Replace processor board
		#	#	/	/	/	/	CPU Error	Replace processor board
	#			/	/	/	/	CPU Error	Replace processor board
	#	#						RAM Error	Replace SIMM card in slot A1
	#	#					#	RAM Error	Replace SIMM card in slot A2
	#	#				#		RAM Error	Replace SIMM card in slot B1
	#	#				#	#	RAM Error	Replace SIMM card in slot B2
	#	#			#			RAM Error	Replace SIMM card in slot C1

	#	#			#		#	RAM Error	Replace SIMM card in slot C2
	#	#			#	#		RAM Error	Replace SIMM card in slot D1
	#	#			#	#	#	RAM Error	Replace SIMM card in slot D2
#		#	#			#		I/O Error	Replace I/O Card
#		#	#		#		#	CPU Error	Replace processor board
#		#	#		#	#		Error	Replace processor board *or* on SIMM
#		#	#		#	#	#	Error	Replace processor board *or* I/O card
#		#	#	#			/	Error	Replace processor board *or* I/O card

2.8.6 735/755

Taken from the Service manual and supplied by Greg Fruth, thanks! Illustration of the LED panel.

means LED is on or flashing, - means LED is off.

The codes mean different things depending on what state the machine is in. There are codes for the Selftest, the PDC (Processor Dependent Code), the ISL (Initial System Loader) and HP-UX (that's the order in which they run). Some of the Selftest LED codes should be listed in your owner's guide.

```
################################################################################
Selftest LED Codes
################################################################################
 LED #
87654321        FRU             Error
================================================================================

---#---#        Processor       CPU Diagnose Register
                Board
---#--#-                        CPU Basic Functions

---#--##                        CPU ALU & Branch

---#-#--                        CPU Arithmetic Conditions

---#-#-#                        CPU Bit Operations

---#-##-                        CPU Arithmetic Side Effects

---#-###                        CPU Control Registcrs

---##---                        CPU External Interrupts

---##--#                        CPU Shadow Registers

---##-##                        TLB Initialization
```

```
--#----#                    Cache Data Line

--#---#-                    Cache Address Line

--#---##                    Instruction Cache RAM

--#--#--                    Data Cache RAM

--#--#-#                    Cache Tag Compare

--#--##-                    Cache Errors

--#--###                    Cache Configuration

--#-#---                    Cache Flush

--#-#--#                    Cache Byte Transaction

--#-#-#-                    Instruction Cache Miss

--#-#-##                    Data Cache Miss

--#-##--                    Cache Done

--##---#                    Memory Interface EIR

--##--#-                    Memory Interface HPMC

--##--##                    Memory Interface

--##-#--                    Memory Interface Invalid Address

--##-#-#                    Memory Interface Single Bit Error

--##-##-                    Memory Interface Double Bit Error

--##-###                    Memory Interface Diagnose Register

-#-----#                    Floating Point Registers

-#----#-                    Floating Point Instructions
```

-#----##		Floating point Traps
-#-#---#	EISA Interface Controller	EISA Init
-#-#--#-		EISA ADDR Test
-#-#--##		ADDR Test Failure
-#-#-#--		EISA Pattern Test
-#-#-#-#		EISA Pattern Test Failure
-#-#####		RAM CHECKSUM Failure
-##-----	Memory	RAM Slot 5B (J100) Error
-##----#		RAM Slot 4B (J102) Error
-##---#-		RAM Slot 3B (J104) Error
-##---##		RAM Slot 2B (J106) Error
-##--#--		RAM Slot 1B (J108) Error
-##--#-#		RAM Slot 0B (J110) Error
-###----		RAM Slot 5A (J101) Error
-###---#		RAM Slot 4A (J103) Error
-###--#-		RAM Slot 3A (J105) Error
-###--##		RAM Slot 2A (J107) Error
-###-#--		RAM Slot 1A (J109) Error
-###-#-#		RAM Slot 0A (Jlll) Error
-###-###		RAM Configuration & Test In Progress

```
-#####-#                        No RAM Found

-######-                        Non-Destructive RAM Test

-#######                        RAM Configuration & Test

#-------        Processor       Unknown I/O Device
               Board
#------#                        Single-Ended SCSI Init

#-----#-                        LAN Init

#-----##                        HIL Init

#----#--                        RS232 Port A Init

#----#-#                        RS232 Port B Init

#----##-                        Parallel Port Init

#---#---        SGC Slot 0      Graphics Init

#---#--#        EISA Card       EISA Slot Init

#--##---        FDDI Slider     FDDI Init
               Board
#--##--#        Processor       Fast Wide SCSI Init
               Board


################################################################################
PDC LED Codes
################################################################################
 LED #
87654321        Status
================================================================================

#-#----#        Destructive Memory Init

#-#---#-        Non-Destructive Memory Init

#-#---##        Console Selection
```

```
#-#--#--        Boot Device Selection

#-#--#-#        Autoselection Failure to Find Boot Device

#-#--##-        Launching IPL

#-#--###        TOC Handler Entered

#-#-#---        Branching to OS TOC Handler

#-#-#--#        Branching to OS HPMC Handler

#-#-#-#-        EISA Subsystem Init

#-#-#-##        Setting Up Default EISA Config

#-#-##-#        At Least One Selftest Failed (Service Mode)

#-##---#        Error Reading EEPROM

#-##--#-        Unexpected Interrupt

#-##--##        No Console Located

#-##-#--        HPMC Handling Init

#-##-#-#        HPMC Due to Cache Error

#-##-##-        HPMC Due to Memory Error

#-##-###        HPMC Due to Bus Error

#-###---        Nested HPMC Detected

#-###--#        Error Writing EEPROM

#-###-#-        Unable to Determine Valid Processor Speed

#-####--        Processor Speed Sensing

#-####-#        Problem Calculating Memory Control Values
```

```
#-######        Bad Memory Hardware


################################################################################
ISL LED Codes
################################################################################
 LED #
87654321        Status
================================================================================

--------        ISL Executing.

-------#        ISL is Autobooting from the Autoexec file.

------#-        ISL Cannot Find Autoexecute file.

------##        No Console Found. ISL Autobooting.

-----#-#        Directory of utilities is too large.

-----##-        Autoexec File is Inconsistent.

---#--#-        Error Reading Autoexec File.

---#--##        Error Reading from Console.

---#-#--        Error Writing to Console.

---#-#-#        Not an ISL Command or Utility.

---#-##-        Utility File Header Inconsistent: Invalid System ID.

---#-###        Error Reading Utility File Header.

---##---        Utility Flle Header Inconsistent: Bad Magic Number.

---##--#        Utility Would Overlay ISL in Memory.

---##-#-        Utility Requires More Memory Than Is Configured.

---##-##        Error Reading Utility Into Memory.
```

```
---###--        Incorrect Checksum: Reading Utiliy Into Memory.

---###-#        System Console Needed.

---####-        Internal Inconsistency: Invalid Boot Device Class.

--#----#        Destination Memory Address of Utility is Invalid.

--#---#-        Internal Inconsistency pdc_cache entry

--#---##        Internal Inconsistency: IODC ENTRY_INIT

--#--#--        Internal Inconsistency: IODC ENTRY_INIT Console

--#--#-#        Internal Inconsistency: IODC ENTRY_INIT Boot Device

--#--##-        Utility File Header Inconsistent: Bad aux_id

--#--###        Bad Utility File Type


################################################################################
HP-UX Kernel LED Codes
################################################################################
 LED #
87654321        Status
================================================================================

###-----        Kernel Loaded and Initialization Begun.

####---#        Kernel Has Entered main().

####--#-        Kernel Is About to Configure I/O System.

####-#--        Kernel Is About to Mount Root File System.

####-##-        Kernel Is About to Set Up Page-Out Daemon.

#####---        Kernel is About to Start the "INIT" Process.

--------        Shutdown In Process.
```

```
-----#--        TOC Dump.

---#----        HPMC Dump.

--#----#        Operating System Executing with Load
                Indicator X.
```

Once the machine is into HP-UX, the top 4 amber LEDs (1-4) assume the meanings given by the hieroglyphics next to the LEDs themselves (i.e. net transmit, net receive, SCSI, heartbeep). The bottom 4 LEDs (5-8) give the system load factor (as reported by "uptime", "w", etc.)

2.8.7 B-Class

Taken from the Owner's Guide. Picture of B-Class front panel with LEDs.

means LED is on or flashing, _ means LED is off.

LED value	RS-232 range	Description
_ _ _ #	7401	No memory found FAULT.
_ _ # #	7000-7F00	Memory Error FAULT. (sys console indicates which board)
_ # _ _	1030-4099	Processor board FAULT.
_ # _ #	5000-500F, 8000-8FFF, CD00-CDFF	I/O System FAULT
_ # # _	8500, 8501, 8C00-8CFF	Backplane FAULT (incl. PCI).
_ # # # # _ _ _	Any	INITIALIZATION and TESTING. (alternating 1000, 0111, ...)
# _ _ #	Any not in this table	Unknown FAULT.
# _ # _	CBF0-CBFF, 1001	HPMC FAULT (very bad).
# # _ #	A088-A0FF	No console/IPL error FAULT.
# # # #		If remains for longer than 1s after power-on: processor board FAULT.

2.8.8 C-Class

Taken from the Service Manual. Picture of C-Class front panel with LEDs.

means LED is on or flashing, _ means LED is off.

LED value	RS-232 range	Description
_ _ _ #	7500	No memory found FAULT.
_ _ # _	7501, 7502	Not enough memory found FAULT.
_ _ # #	7000-7D0A	Processor Board/Memory Error FAULT. (sys console indicates which board)
_ # _ _	1030-4071	Processor board FAULT.
_ # _ #	5000-500F, 8000-8FFF, CD00-CDFF	I/O System FAULT
_ # # _	CD1E, CDEF, CDD0	Backplane FAULT (incl. PCI).
_ # # # # _ _ _	Any	INITIALIZATION and TESTING. (alternating 1000, 0111, ...)
# _ _ #	Any not in this table	Unknown FAULT.

# _ # _	CBF0-CBFF, 1001	HPMC FAULT (very bad).
# # _ #	A000-A0C0	No console/IPL error FAULT.
# # # #		If remains for longer than 1s after power-on: processor board FAULT.

2.9 PA-RISC Graphics Adapters

2.9.1 Overview

An attempt to describe at least the basic details of the most common HP graphics adapters.

2.9.2 CRX

CRX graphics adapters were available in various different configurations for both the SGC and GSC bus in their different formfactors. All of these adapters were officially only supported in HP-UX up to 10.20, some may still work with 11.00.

They output a fixed resolution of **1280x1024** the SGC-cards in the DIO-II formfactor use one (grayscale), three (RGB) or four (RGB+sync) BNC-connectors, while the SGC and GSC cards in the EISA formfactor and the mainboard-integrated CRX-adapters use standard HD15 VGA connectors.

Multiple entries for one adapter list the different visuals which can be used when using HP's X11-server (ie. under HP-UX with a graphical interface).

Device	max. color-depth	Colormaps	Overlay	Double-buffering	HW Z-buffer/ 3D-accel.	Bus/Formfactor: Part-number
GRX	8-bit grayscale	1	-	software	-	SGC (DIO-II): A1924A
CRX	8-bit	2	-	hardware	-	SGC (DIO-II): A1659A
Stinger (CRX) *(See Note 1)*	8-bit	2	-	software	-	SGC (integrated)
Artist (CRX) *(See Note 2)*	8-bit	2	-	hardware	-	GSC (integrated)
CRX-24	8-bit	3	-	hardware	-	SGC (DIO-II FF): A1439A SGC (EISA FF): A2673A
	8-bit	3	8-bit	software	-	
	12-bit	1	-	hardware	-	
	24-bit	1	-	-	-	
CRX-24Z *(See Note 3)*	24-bit	1	-	-	yes	SGC (DIO-II FF): A1454A SGC (EISA FF): A2674A
CRX-48Z *(See Note 4)*	8-bit	1	-	hardware	-	SGC (DIO-II FF) + ext.: A2091A SGC (EISA FF) + ext.: A2675A GSC (EISA FF) + ext.: A4073A/B + A4074A
	8-bit	1	8-bit	software	-	
	24-bit	1	-	hardware	yes	

Notes

1. The *Stinger* CRX-adapter, integrated into some of the older ASP-based workstations (older 715, 725) supports four different resolution/refresh-rate combinations, which can be changed via a DIP-switch on the back of the machine or in the PDC.

2. The Artist graphics adapter, as found on many LASI-based workstations, is technically identical to the CRX devices but supports much more resolutions and refresh rates, which can be chosen in the boot-ROM.

3. The **Z**-suffix denotes a CRX-board with an optional 3D-acceleration board, containing a hardware 24-bit Z-buffer. These combined adapters (e.g. CRX-24Z) can be used with the same visuals as stand-alone versions (e.g. CRX-24) but always provide the 3D-acceleration. The hardware acceleration can only be used in conjunction with the Starbase, PHIGS, PowerShade or PEX APIs.

4. The CRX-48Z adapter actually consists of a GSC or SGC interface card and a separate external processing box, which connects to the interface card and provides the RGB output connectors.

2.9.3 HCRX

Successors to the CRX graphics adapters, found only in systems with the GSC bus, either integrated into the main logic or as a separate expansion board.

They output a fixed resolution of **1280x1024** and use a standard HD15 VGA connector.

Multiple entries for one adapter list the different visuals which can be used when using HP's X11-server (ie. under HP-UX with a graphical interface).

Device	max. color-depth	Colormaps	Overlay	Double-buffering	HW Z-buffer/ 3D-accel.	Bus/Formfactor: Part-number
HCRX-8	8-bit	2	-	hardware	-	GSC (EISA FF): A4070A/A4070B GSC (GSC-M FF): A4315A
	8-bit	2 + 2 (ov.)	8-bit	software	-	
HCRX-8Z *(See Note 1)*	8-bit	2	-	%	yes	GSC (EISA FF): A4079A/A4079B
HCRX-24	8-bit	2	-	hardware	-	GSC (EISA FF): A4071A/A4071B GSC (GSC-M FF): A4316A
	8-bit	2 + 2 (ov.)	8-bit	software	-	
	12-bit	1	-	hardware	-	
	24-bit	1	-	-	-	
HCRX-24Z *(See Note 1)*	24-bit	1	-	%	yes	GSC (EISA FF): A4179A

Notes

1. The **Z**-suffix denotes a HCRX-board with an optional 3D-acceleration board, containing a hardware 24-bit Z-buffer. These combined adapters (e.g. HCRX-24Z) can be used with the same visuals as stand-alone versions (e.g. HCRX-24) but always provide the 3D-acceleration. The hardware acceleration can only be used in conjunction with the Starbase, PHIGS, PowerShade or PEX APIs.

2.9.4 Visualize

The HP Visualize line of graphics adapters were used in a large number of PA-RISC workstations (integrated onto the mainboard) and expansion cards of various types. All cards provide 2D hardware acceleration which is used in HP's X-server, the 3D hardware acceleration can only be used in conjunction with the Starbase, PHIGS, PowerShade or PEX APIs.

They use either a standard HD15 VGA or EVC connector.

Multiple entries for one adapter list the different visuals which can be used when using HP's X11-server (ie. under HP-UX with a graphical interface).

Device	**max. resolution**	**max. colordepth**	**Colormaps**	**Overlay**	**Double-buffering**	**HW Z-buffer/ 3D-accel.**	**Bus/Formfactor: Part-number**
Visualize-EG (base)	1280x1024	8-bit	2	-	software	-	GSC (EISA FF): A4450A GSC (HSC FF): A3519A PCI: A4977A PMC (PCI mezzanine): A4979A
Visualize-EG (dual)	1280x1024	8-bit	2	-	software	-	GSC (EISA FF): A4451A
Visualize-EG (ext. mem)	1280x1024	8-bit	2 + 2 (ov.)	8-bit	software	-	GSC (EISA-FF): + A4452A
	1600x1200	8-bit	2	-	hardware	-	
Visualize-8	1280x1024	8-bit	2	-	hardware	yes	GSC (EISA FF): A4441A
		8-bit	2 + 2 (ov.)	8-bit	software	yes	
Visualize-24	1280x1024	8-bit	2	-	hardware	yes	GSC (EISA FF): A4442A
		8-bit	2 + 2 (ov.)	8-bit	software	yes	
		12-bit	1	-	hardware	yes	
		24-bit	1	-	-	yes	

Visualize-48	1280x1024	8-bit	4	-	hardware	yes	GSC (EISA FF): A4244A
		8-bit	4 + 2 (ov.)	8-bit	software	yes	
		24-bit	4	-	hardware	yes	
Visualize-48XP	1280x1024	8-bit	4	-	hardware	yes	GSC (2-slot EISA FF): A4246A GSC (HSC FF): A4455A
		8-bit	4 + 2 (ov.)	8-bit	software	yes	
		24-bit	4	-	hardware	yes	

2.9.5 Visualize-FX

The HP Visualize-FX graphics adapters were a more or less complete redesign in contrast to their Visualize predecessors. The architecture of the graphics processors is PA-RISC based, the higher-end models in fact include more than four PA-RISC CPUs to process the graphics. The **FX**s were the first HP cards to support the OpenGL X-Window Extension (GLX), in addition to the legacy 3D APIs (Starbase, PEX, PHIGS). These adapters were only available as PCI-bus cards, with some using two slots.

The EVC connector present on some cards needs an adapter cable (about $20) to connect to a standard HD15 VGA monitor.

These cards support a maximum resolution of **1600x1200**, although only with a proper VESA monitor. Otherwise they support **1280x1024**. Both Sync-on-Green and Digital-Sync output signals aresupported.

Multiple entries for one adapter list the different visuals which can be used when using HP's X11-server (ie. under HP-UX with a graphical interface).

Device	**max. color-depth**	**Colormaps**	**Overlay**	**Double-buffering**	**HW Z-buffer/ 3D-accel.**	**Output**	**Bus/Formfactor: Part-number**
Visualize-FXE	8-bit	2	-	hardware	yes	VGA	PCI 32-bit 66MHz: A4982A *(See Note 1)*, A4982B *(See Note 1)*
	8-bit	2 + 2 (ov.)	8-bit	software	yes		
	24-bit	2	-	hardware	yes		
Visualize-FX2	8-bit	4	-	hardware	yes	EVC	PCI 64-bit 66MHz: A4552A
	8-bit	4 + 2 (ov.)	8-bit	software	yes		
	12-bit	2	-	hardware	yes		
	24-bit	4	-	-	yes		

Visualize-FX4/FX6 *(See Note 2)*	8-bit	4	-	hardware	yes	EVC	PCI 64-bit 66MHz: A4553A (FX4) PCI 64-bit 66MHz: A4554A (FX6)
	8-bit	4 + 2 (ov.)	8-bit	software	yes		
	12-bit	2	-	hardware	yes		
	24-bit	4	-	hardware	yes		
Visualize-FX5/FX10	8-bit	2	-	hardware	yes	VGA, DVI-D, stereo	PCI 64-bit 66MHz: A1264A (FX5) *(See Note 3)* PCI 64-bit 66MHz: A1264B (FX5pro) *(See Note 3)* PCI 64-bit 66MHz: A1298A (FX10) *(See Note 3)* PCI 64-bit 66MHz: A1298B (FX10pro) *(See Note 3)*
	8-bit	2 + 2 (ov.)	8-bit	software	yes		
	24-bit	2	-	hardware	yes		

Notes

1. There were two FXE models with different memory subsystems for unified buffer, Z-buffer and texture storage:

   - A4982A: 18MB SGRAM, (3.5MB max for textures)
   - A4982B: 24MB SDRAM, (9.5MB max for textures)

   The **A**-version is a bit faster due to used SGRAM.

2. The FX4 and FX6 card support an optional 16MB hardware texture memory module.

3. The FX5/10**pro** models integrate the raster and texture-processor into a single IC, resulting in a better performance than the standard FX5/10 models. The onboard RAM is used as unified buffer, Z-buffer and texture storage:

- FX5[pro]: 64MB (48MB max. for textures)
- FX10[pro]: 128MB (110MB max. for textures)

2.9.6 FireGL-UX

This high-end graphics adapter is based on the popular ATI FireGL2 board, available for x86-PCs. It provides full OpenGL hardware acceleration under HP's X-Server and is binary compatible with the Visualize FX10pro adapter.

- IBM GT1000 geometry engine
- IBM RC1000 raster engine
- 128MB DDR SDRAM of unified frame buffer, Z-buffer and texture storage
- Digital DVI and 3-pin stereo output
- Only available as 64-bit, 66MHz PCI-card

It is about twice as fast as the Visualize FX10pro.
Supported resolutions and refresh rates:

Resolution	Refresh rate	Color depth
640x480	100Hz	24-bit
800x600	100Hz	24-bit
1024x768	100Hz	24-bit
1152x864	100Hz	24-bit
1280x960	100Hz	24-bit
1280x1024	100Hz	24-bit
1600x1000	85Hz	24-bit
1600x1024	85Hz	24-bit
1600x1200	85Hz	24-bit
1792x1344	60Hz	24-bit
1920x1200	76Hz	24-bit

2.9.7 References

- **HP-UX Graphics Administration Guide**[37]

[37] http://docs.hp.com/hpux/onlinedocs/B2355-90142/B2355-90142.html

2.10 PA-RISC SCSI

2.10.1 SCSI Bus

The below table lists some of the incarnations of the SCSI-bus as found in PA-RISC computers.

SCSI	**Clock**	**Width**	**max data rate**	**max devices** *(See Note 1)*	**Signals** *(See Note 2)*	**max length**	**Connector**
Narrow SCSI	5MHz	8-bit	5MB/s	7	SE	6m	50-pin
Fast-Narrow SCSI	10MHz	8-bit	10MB/s	7	SE	3m	50-pin
					HVD	25m	
Fast-Wide SCSI	10MHz	16-bit	20MB/s	15	SE	3m	68-pin
					HVD	25m	
Ultra-Narrow SCSI	20MHz	8-bit	20MB/s	7	SE	1.5m	50-pin
					LVD	12m	
					HVD	25m	
Ultra-Wide SCSI	20MHz	16-bit	40MB/s	15	SE	1.5m	68-pin
					LVD	12m	
					HVD	25m	
Ultra2-Wide SCSI	40MHz	16-bit	80MB/s	15	LVD	12m	68-pin
Ultra160 SCSI	40MHz	16-bit	160MB/s	15	LVD	12m	68-pin
Ultra320 SCSI	80MHz	16-bit	320MB/s	15	LVD	12m	68-pin

Notes

1. excluding the SCSI-hostadapter.
2.
   - SE - Single-Ended
   - HVD - High-Voltage Differential
   - LVD - Low-Voltage Differential

2.10.2 SCSI Chips

A listing of the common SCSI chips used in some of the PA-RISC based workstations and servers from HP. These chips were both integrated into the main-logic of these systems and available on plug-in cards.

53C700

Used in

- 705 & 710
- 715/{33,50,75}
- 725/{50,75}
- 720, 730, 750
- 735, 755 (*ASP2*)
- 742i/50
- 745i/{50,100}
- 747i/{50,100}

The 53C700 is the primary SCSI-controller of the very early PA-RISC workstations which include the ASP-chipset. It only supports 5MHz narrow-transfers.

Features

- one narrow SCSI channel
- chip support for SE transfer modes
- synchronous SCSI transfer rate of 5MB/s

53C710

Used in

- 712/{60,80,100}
- 715/{64,80,100}
- 725/100
- 743i/{64,100}
- 744/{132L,165L}
- 748i/{64,100,132L,165L}
- A180, A180C
- B132L, B132L+, B160L, B180L+
- C100, C110, C132L, C160L, C160, C180, C200, C240, C360
- D-Class
- E25, E35, E45, E55
- J200, J210, J210XC, J280, J282
- K-Class
- RDI PrecisionBook 132, 160, 180
- R380, R390
- SAIC Galaxy 1100

The NCR 53C710 was the primary SCSI controller used in the early, post-ASP HP 9000s. Integrated in the LASI ASIC as a macrocell, all of the above named workstations used this implementation as the controller for their 8-bit SE SCSI-2 bus.

Features

- one Fast-Narrow SCSI channel
- chip support for SE and HVD transfer modes (in the HP 9000s only SE logic is used)
- synchronous SCSI transfer rate of 10MB/s
- asynchronous SCSI transfer rate of over 5MB/s
- 64-Byte DMA FIFO
- bus master DMA device
- attaches to host bus interface, can either be Motorola 68030 (bus up to 25MHz async) or 68040 (bus up to 33MHz sync) compatible
- sustained host bus bandwidth of up to 42.66MB/s

53C720

Used in

- 735, 755 (*ASP2*)
- B132L, B160L
- C100, C110, C132L, C160L, C160, C180
- D-Class
- J200, J210, J210XC, J280, J282
- K-Class
- R380, R390

The NCR 53C720 was the secondary SCSI controller used in the early HP 9000s for the attachment of an Fast-Wide (16-bit) SCSI-2 bus, utilizing HVD signalling. It was either controlled by the ASP2 chipset or interfaced to the GSC bus through a chip named Zalon.

Features

- one Fast-Wide SCSI channel
- chip support for SE and HVD transfer modes (in the HP 9000s only HVD logic is used)
- synchronous SCSI transfer rate of 20MB/s
- asynchronous SCSI transfer rate of 10MB/s
- 64-Byte DMA FIFO
- 16- or 32-bit bus master DMA device

- attaches to host bus interface, can either be Motorola 68030 (bus up to 25MHz async) or 68040 (bus up to 33MHz sync) or Intel 80386SX or 80386DX compatible
- support both big or little endian
- sustained host bus bandwitdh of more than 100MB/s
- 208-pin QFP package

53C875

Used in

- A400 (rp2400, rp2430), A500 (rp2450, rp2470)
- B132L+, B180L+
- C200, C240, C360
- L1000 (rp5400), L2000 (rp5450)
- N4000
- Superdome
- V2200, V2250

The Symbios Logic/LSI 53C875 is the chip that provides the single Ultra-Wide SE SCSI channel on some of the newer PA-RISC workstations.

Features

- one Ultra-Wide SCSI channel
- chip support for SE transfer modes
- synchronous SCSI transfer rate of 40MB/s
- asynchronous SCSI transfer rate of 14MB/s
- 4KB SCRIPTS RAM
- 536-Byte DMA FIFO
- 20MHz SCSI clock
- attaches to 32-bit, 33MHz PCI (PCI-32/33), both 3.3V or 5V
- 160-pin PQFP or 169-pin PBGA package

References

- **LSI 53C875E**[38] (PDF, 0.3MB)

[38] http://www.lsilogic.com/files/docs/marketing_docs/storage_stand_prod/raid/lsi53c875e_pb.pdf

53C896

Used in

- A400 (rp2400, rp2430), A500 (rp2450, rp2470)
- B1000, B2000, B2600
- C3000, C3600, C3700
- J5000, J5600, J6000, J6700, J7000, J7600
- L1000 (rp5400), L2000 (rp5450)

The Symbios Logic 53C896 SCSI ASIC is the chip used on some of the newer PA-RISC workstations and servers to control their storage I/O buses. This ASIC includes two 53C895-equivalent cores to control the two internal channels separately.

Features

- two independent Ultra2-Wide SCSI-3 channels
- chip support for LVD, HVD and SE transfer modes
- synchronous SCSI transfer rate of 80MB/s for each channel
- integrated LVDlink SCSI transceivers
- 8KB SCRIPTS RAM for each channel
- 944-Byte DMA FIFO for each channel
- 40MHz SCSI clock
- attaches to 64-bit, 33MHz PCI (PCI-64/33)
- 329-pin PBGA package

References

- **LSI 53C896**[39] (PDF, 0.2MB)

2.10.3 SCSI Adapters

SCSI adapters (HBAs) for the various expansion buses found in PA-RISC systems.

EISA

SCSI adapters for the EISA bus.

Part-no.	SCSI type	Signalling *(See Note 1)*	Boot	HP-UX
A2679A	Fast-Narrow	SE	no	9.0-11i/32-bit
25525A	Fast-Narrow	HVD		8.05-10.20
25525B	Fast-Narrow	HVD		8.05-11.0/32-bit

[39] http://www.lsilogic.com/files/docs/marketing_docs/storage_stand_prod/raid/lsi53c896_pb.pdf

GSC

SCSI adapters for the various incarnations of the GSC bus.

Part-no.	GSC formfactor	SCSI type	Signalling *(See Note 1)*	Boot	HP-UX
A2874-66005	EISA	Fast-Wide	HVD	yes	9.05/11.0
A2969A	HSC	Fast-Wide	HVD	yes	10.01-11i
A3644A *(See Note 2)*	HSC	Fast-Wide	HVD		10.20-11i
A4107A	EISA	Fast-Wide	HVD		9.05-11i/32-bit
A4268A	GSC-M	Fast-Wide	HVD	yes	9.05-11.0/32-bit

HP-PB

SCSI adapters for the various incarnations of the HP-PB bus.

Part-no.	SCSI type	Signalling *(See Note 1)*	Boot	HP-UX
27251A				
28655A	Fast-Narrow	SE	yes	10.01-11i
28696A	Fast-Wide	HVD	yes	10.01-11i

PCI

SCSI adapters for the various incarnations of the PCI bus.

Part-no.	SCSI type	Signalling *(See Note 1)*	Boot	HP-UX
A4800A	Fast-Wide	HVD	yes	10.2-11i
A4974A	Ultra-Wide	SE	yes	10.20-11.0
A4976A	Fast-Wide	HVD	yes	10.20-11.0
A4999A	Ultra2-Wide	LVD	yes	10.20-11.0
A5159A	Fast-Wide	HVD	yes	10.20-11i

Notes

1.
   - SE - Single-Ended
   - HVD - High-Voltage Differential
   - LVD - Low-Voltage Differential
2. This card is only supported in the T-Class

Chapter 3

PA-RISC Operating Systems

3.1 HP-UX

3.1.1 Overview

HP-UX is HP's implementation of Unix. It was first released in 1986, and ran at that time on the HP 9000/500 series driven by HP FOCUS CPUs.

HP-UX up to version 9.x was an Unix with a very strong BSD-flavour (and supposedly very similar to HPBSD), from 10.x onwards the system got more and more SystemV-style. Up to version 10.x there were different releases for the HP 9000/700 workstations and 800 servers, each ones needed different install media though programs compiled on either would also run on the other.

HP-UX 10.20 was a very popular version, since it runs quite smoothly on older systems and was generally a very unbloated release with support for most of the distributed hardware. Due to the supposed Y2K-problems of HP-UX versions <10.x HP decided to make a free 10.20 upgrade media set available for all owners of an 700 workstation (not 800s server though).

From version 11.00 onwards, identical media and releases could be used for the 700s and 800s, the two main 11-releases are 11.00 and 11.11 (a.k.a. 11i). These version are quite a dog on older systems and even newer ones require a good amount of RAM to work smoothly. 11.x was also supposedly the first true 64-bit version of HP-UX, it supported the full 64-bit features of machines based on PA-8x00 64-bit CPUs.

3.1.2 HP-UX 10.20 for 700s

It is reasonably fast on all machines with at least 64MB RAM. If you're planning to use CDE or want to bring the system under heavy load, more than 128MB is always a wise decision. With the introduction of 10.20 HP-UX shifted to a more *System V-like* Unix, in contrast to version up to 9.x, which was stronger *BSD*-flavoured. HP-UX 10.20 is pretty straightforward to configure and install. After booting the CD media you'll get to the *swinstaller* which takes you by the hand while installing. After the installation *SAM*'ll be your friend. Almost all sysadmin duties can be carried out with this tool, like adding devices, configuring the kernel, X-server, network and mounting filesystems.

System requirements

- HP-UX 10.20 runs on most available PA-RISC systems, however some of the newer 64-bit are not supported.
- it needs from 300MB (without X11) up to 800MB (fullblown) diskspace
- 64MB RAM minimum, 128 (or more) are better
- all available HP graphics options are supported
- all available HP input devices are supported

References

- Installation instructions can be found in HP's B2355-90173 document available at docs.hp.com as **PDF**[1] (2.1MB) and **HTML**[2].

  Chapter 2[3] is the start of the installation instructions.

3.1.3 HP-UX 10.20 for 800s

This version of HP-UX includes special device drivers and other components specific to Series 800 systems. This release should run on most PA-RISC servers with at least a PA-7000 CPU. Similarly to the 700s release, some newer 64-bit systems are not supported. 64MB of RAM should be the minimum amount to get the system running, more is probably better.

3.1.4 HP-UX 11.00

Version 11.00 is HP's first Unix to implement a full 64-bit kernel. Nevertheless, it still runs on a number of systems featuring a 32-bit CPU. All HP 9000/800 servers with at least a PA-7000 should be supported, although some expansion options have been discontinued for those systems. *Official* support for HP 9000/700 workstations was only continued for those systems featuring at least a PA-7100LC CPU. With careful review of the newer OS patches older systems with e.g. PA-7100 and PA-7150 CPUs can also be made to run 11.00.

The last 11.00 HP-UX version reported to run on 735 and 755 should be from March 2000. This also means that the latest "HP-UX General Release Patches" that do not hose the 735/755 are also from March 2000.

11.00 can run in either 64-bit or 32-bit mode on systems with a PA2.0 CPU (e.g. at least PA-8000) or in pure 32-bit mode on all PA1.1 CPUs.

System requirements

- it needs from 500MB up to 1000MB (fullbloated) diskspace
- system should have at least 128MB of RAM; with CDE >256MB is far better
- all available HP input devices are supported
- GRX and CRX (CRX-8, [H]CRX-24[Z], [H]CRX-48-[Z] are not supported
- several EISA expansion cards and all HP-IB interfaces are not suppored anymore

References

- Installation instructions can be found in HP's B2355-90163 document available at docs.hp.com as **PDF**[4] (4.1MB) and **HTML**[5].

[1] http://docs.hp.com/hpux/pdf/B2355-90173.pdf
[2] http://docs.hp.com/hpux/onlinedocs/B2355-90173/B2355-90173.html
[3] http://docs.hp.com/hpux/onlinedocs/B2355-90173/00/00/12-con.html
[4] http://docs.hp.com/hpux/pdf/B2355-90153.pdf
[5] http://docs.hp.com/hpux/onlinedocs/B2355-90153/B2355-90153.html

Booting the target System[6] is the start of the installation instructions.

- **Building a Bastion Host Using HP-UX 11**[7] is also a good reference for installing and later on trimming down HP-UX.

3.1.5 HP-UX 11i (11.11)

Version 11i (or 11.11) is the latest HP-UX release for PA-RISC based computers and extends the hardware support from 11.00 to more high-end systems as e.g. SuperDome featuring up to 128 CPUs. As this is the current active HP-UX release most patches and available software is geared towards 11i.

With the release of this version the concepts of different Operating Environments (OEs) was introduced to target systems with different roles with appropriate software and OS collections. The HP-UX 11i Operating Environment (OE) is the smallest collection for normal workstations and servers. It is a subset of the Enterprise Operating Environment (TOE) which contains software and features aimed at larger servers. This in fact is again a subset of the Mission Critical Operating Environment (MCOE), which contains even more software needed for building large clusters and server systems. Another set are the Technical Operating environments, aimed at workstations for CAD/CAM and development uses. The smallest set is the Minimal Technical Operating Environment (MTOE) which in fact is a subset of the Technical Computing Operating Environment (TCOE) which contains more software for development purposes. The OEs are available as CD sets but can be installed via an Ignite-UX server. The 11i CD sets are made available bi-annually, newer releases always include the at that point actual patch sets and software enhancements.

System requirements

The list of officially supported systems was reduced even further compared to 11.00, the support for older systems was phased out in favour of new systems and hardware devices. The support matrices from HP in the References section below state which systems are officially supported; the [computers] index page and the particular model pages here in turn list which HP-UX releases are known to work, even if unsupported. In most cases officially unsupported systems are able to run 11i, though sometimes installing can be complicated. It is also needed to carefully review the OS patches on older systems as some SCSI patches can break the system. Since some newer release already contain these patches older 11i release have to be used for some of these older systems.

11i generally has the same requirements as 11.00, although 256MB of RAM is the bare minimum for a graphical environment. Some systems though run faster with 11i then e.g. with 11.00.

It has to be noted that some I/O-subsystems and devices aren't supported anymore in 11i.

References

- Many useful documents relating HP-UX 11i can be found at **http://docs.hp.com/hpux/os/11i**[8].

[6] http://docs.hp.com/hpux/onlinedocs/B2355-90153/00/00/19-con.html
[7] http://secinf.net/unix_security/Building_a_Bastion_Host_Using_HPUX_11.html
[8] http://docs.hp.com/hpux/os/11i/index.html

- The **hp-ux 11i operating environments**[9] (PDF, 3.8MB) document explains in greater detail the different available OEs.
- Installation instructions can be found in HP's 5990-7279 document available at docs.hp.com as **PDF**[10] (4.1MB) and **HTML**[11].
- The **Release Notes**[12] for the various 11i release each list the supported hardware and software configurations.
- **Building a Bastion Host Using HP-UX 11**[13] is also a good reference for installing and later on trimming down HP-UX (and should also apply to 11i).

3.1.6 Software for HP-UX

- The **Software Porting And Archive Centre for HP-UX**[14] has some precompiled binaries for both 10.20 and 11. (They used to have more!)
- Selected software for 10.20, including gcc-3, can be found at **The Written Word FTP**[15].
- Same as above for 11.00, including gcc-3, can be found at **The Written Word FTP**[16].
- HP's **software depot home**[17] offers a lot of software from different categories for download (mostly free of charge).
- The **DSPP developer edge**[18] ("developer & solution partner program") from HP contains various resources fo HP-UX developers.
- **Managing HP-UX Software With SD-UX**[19] from docs.hp.com gives a very good overview and lots of details on how to install/manage software on a HP-UX system using sdinstall/swinstall.

3.1.7 References

- The **HP-UX FAQ**[20] has lots of useful info.
- If you want to know details of HP-UX and Unix-commands HP has the **HP-UX manual pages**[21] on the web.
- The **Unix update support matrix**[22] from HP notes each supported OS version for every workstation model.

[9] http://docs.hp.com/hpux/onlinedocs/os/11i/hpwoldfullpres.pdf
[10] http://docs.hp.com/hpux/pdf/5990-7279.pdf
[11] http://docs.hp.com/hpux/onlinedocs/5990-7279/5990-7279.html
[12] http://docs.hp.com/hpux/os/11i/index.html#ReleaseNotes
[13] http://secinf.net/unix_security/Building_a_Bastion_Host_Using_HPUX_11.html
[14] http://hpux.asknet.de
[15] ftp://ftp.thewrittenword.com/packages/by-architecture/hppa1.1-hp-hpux10.20/
[16] ftp://ftp.thewrittenword.com/packages/by-architecture/hppa1.1-hp-hpux11.00/
[17] http://www.software.hp.com/
[18] http://h21007.www2.hp.com/dev/
[19] http://www.docs.hp.com/hpux/onlinedocs/B2355-90154/B2355-90154_top.html
[20] ftp://rtfm.mit.edu/pub/faqs/hp/hpux-faq
[21] http://www.docs.hp.com/hpux/os/man_pages.html
[22] http://www.hp.com/workstations/risc/standard/operating/support_matrix/update.html

- **HP-UX version and server model support matrix**[23] shows which of the 800s servers are supported under which HP-UX version.
- The **http://www.ussg.iu.edu/usail/installation/hp/hp-install.html**[24] document contains useful info for installing HP-UX.

[23] http://devrsrc1.external.hp.com/STK/serversupport.html
[24] http://www.ussg.iu.edu/usail/installation/hp/hp-install.html

3.2 PA-RISC Linux

3.2.1 Overview

The Linux port to PA-RISC was started by 'The Puffin Group' in November, 1998. By March 1999, HP started helping with equipment and more importantly, documentation.

Because of HP's assistance, the machines targeted were newer than what other ports (e.g. OpenBSD or mklinux) supported like the A180, B180 and 64-bit PA 2.0 systems. Nevertheless, parisc-linux also supports older HP 9000/700 systems like 712, 715 and 735.

3.2.2 Supported hardware

There is generally very broad support for the different PA-RISC systems in PA-RISC Linux. Most of the 'unlettered' (i.e. the 700s) and the B/C/J-Class workstations are supported, both 32-bit (based on PA-7x00 processors) and 64-bit (PA-8x00) systems use the same distribution. SMP is supported, though not as smooth as on other Linux platforms or HP-UX and not necessarily with the theoretical (hardware) maximum of CPUs. PA-RISC Linux runs on most of the server systems, although several of those use more proprietary (weird) I/O and CPU/Memory-combinations and as such are unsupported.

Officially supported systems

- 712/{60,80,100}
- 715/{33,50,75}, 715/{64,80,100}
- 725/{50,75,100}
- 735/{99,125}
- 742i/50
- 743i/{64,100}
- 744/{132L,165L}
- 745i/{50,100}
- 745/{132L,165L}
- 747i/{50,100}
- 748i/{64,100}, 748/{132L,165L}
- 755/{99,125}
- A180[C]
- B132L, B160L, B132L+, B180L+, B1000, B2000, B2600
- J200, J210[XC], J280, J282, J2240, J5000, J6000, J6700, J7000
- C100, C110,C132L, C160L, C160, C180, C200, C240, C360
- D220, D230, D320, D330
- RDI PrecisionBook
- SAIC Galaxy 1100

Most I/O-subsystems are supported, including many of the common PC expansion possibilities. Correct X11 (i.e. graphical) support is confined to a small set of HP adapters and some kind of framebuffer device. Unsupported are most notably the Fast-Wide SCSI, FDDI and audio subsystems on the older ASP-based systems (i.e. 735 and 755 et al). As the more modern machines are more PC-like, support is generally better but still lacking in some delicate areas.

Performance is not quite up to the standards of original HP-UX; 50% is a fair rough estimate of the relative raw performance, although the overhead of a complete running HP-UX probably eats up much of this advantage, especially on slower systems.

3.2.3 Development

In the late 1990s PA-RISC was more or less the last 'big' RISC/Unix architecture without a proper Linux port (besides the limited useful MkLinux and even more limited Mach4/Lites). There were supposedly multiple reasons for this, as the PA-RISC systems were not widely seen at academic entities and had their market share more in the technical/industrial space, from which they did no escape for a long time to a broader userbase. Another fact was that HP was only reluctantly releasing technical documentation on their systems to the general public, even more limiting the target audience of PA-RISC. A function of this closedness and confinement to industrial circles was a very limited hobbyist circle for PA-RISC, as the available machines just were not well documented and more or less witout an available operating system to the private enduser (as compared to the more popular Sun SPARC systems). Slow progress was then made around 1999 with the initial start of the original Linux kernel on PA-RISC, as there seemed to be an growing interest in these machines (as more made their way into the second-hand market), and finally more and more documentation was released.

PA-RISC Linux/Puffingroup

The primary center of (kernel and toolchain) development is the offical **PA-RISC Linux project**[25]. They host a great range of resources, including access to the source code via CVS and CVSWeb, mailing lists for users and developers, installation instructions, an extensive array of documentation and a very useful hardware database.

Early work started in 1999 with the help of The Puffin Group, later employing several kernel and toolchain hackers. Development was at first directed towards 32-bit systems, later on, also through the help of Hewlett Packard, more modern machines were made available to developers, resulting in generally broader hardware and 64-bit support. Parts of the kernel PA-RISC support (most of the trickier ones) were written by HP employees participating in the project. The PA-RISC Linux affiliations changed throughout the last years, HP and developer support fluctuated but the port now reached a very stable state.

ESIEE

(*Contributed by Thibaut Varene*)

[25] http://parisc-linux.org

The PA-RISC Linux port effort started at **ESIEE**[26] in December 1999, with Thierry Simonnet (who was then managing the General IT Resources Service at ESIEE) getting involved in the early stages of the port. By mid September 2000, Simonnet decided to get students involved, and he started a case study for students to participate in as part of their school curriculum. The study was conducted in parallel by HP Labs, who massively sponsored the effort of the school, being one of its long time key partner. This enabled the students to rapidly acquire skills and credibility, and the study was completed in February 2001, and presented at Linux Expo in Paris, and several months later at the Debian 1 Conference in Bordeaux, France. With its increasing success, the initial case study spawned into a larger project that was open to students either on their free time or as part of their classes, and more of them joined what was to be called the PATeam. From 2001 to the end of 2003, the team has been very active, doing numbers of development in the Linux kernel (writing drivers and improving overall stability).

Unfortunately, in 2004 and thereafter, ESIEE gradually reduced its support for the project, and nowadays it doesn't support it anymore, save for website and machines hosting.

3.2.4 Distributions

As of late 2005 there are two popular Linux distributions that include the PA-RISC port: Debian and Gentoo.

Debian

Debian[27] includes PA-RISC Linux as **Debian/hppa**[28] in the 3.1 (aka 'sarge') and 3.0 (aka 'woody') releases. CDs can be ordered as media or downloaded as ISO-images from several **Debian FTP mirrors**[29] in the `3.1_*/hppa` (or *3.0_*/hppa*) directories.

Gentoo

Gentoo[30] was the second distribution which included a **PA-RISC port**[31]. Gentoo is completely compiled from source and uses a BSD-style ports system.

3.2.5 References

- **PA-RISC Linux: HARDWARE SUPPORT**[32] General, textual description of the supported hardware. The PARISC-Linux Project (May 2005).
- **ESIEE PA/Linux Detailed Hardware Support**[33] Detailed status listing with further references. ESIEE The PA/Linux Team (October 2005).

[26] http://www.esiee.fr
[27] http://www.debian.org/
[28] http://www.debian.org/ports/hppa/
[29] http://ftp.ie.debian.org/debian-cd/
[30] http://www.gentoo.org
[31] http://www.gentoo.org/doc/en/handbook/handbook-hppa.xml
[32] http://parisc-linux.org/hardware/supported.html
[33] http://www.pateam.org/list.html

- **Linux on PA-RISC. One Martini Too Many**[34] (PDF, 80KB) Paper for OLS2000 on the early state of the PA-RISC Linux port. Matthew Wilcox (July 2000).

[34] http://ftp.parisc-linux.org/docs/willy/ols2.pdf

3.3 NetBSD/hp700

3.3.1 Overview

Work on a port of NetBSD to PA-RISC 1.x systems was started several times over the last years and brought to shape based on a current OpenBSD kernel in 2004/2005.

The port focuses on **32-bit** PA-RISC 1.1 computers (based on PA-7100, PA-7100LC and PA-7300LC CPUs).

NetBSD/hp700 is only available via so-called binary snapshots, there is no formal release available for this architecture, underlining that the system is still in a very fluctuating state.

3.3.2 Supported Systems

- 712/{60,80,100}
- 715/{33,50,75}
- 715/{64,80,100}
- 725/{50,75}
- 725/100
- 735/{99,125}
- 755/{99,125}
- A180[C]
- B132L, B160L
- B132L+, B180L+
- C132L, C160L
- RDI PrecisionBook

3.3.3 Supported hardware

Buses and Chipsets

All PCI and GSC buses and onboard bus-controllers (ASP, LASI, Dino/Cujo) on the above machines are supported.

The ISA/EISA, Cardbus and HP-PB buses and bus-controllers are not supported.

Networking

All on-board Ethernet and Fast-Ethernet network interfaces on any of the above machines are supported; the FDDI-sliders on the 735/755 are not supported. Expansion cards for the GSC/HSC and PCI-bus slots with a supported Ethernet chipset (Intel i82596, DEC 21142/43 *Tulip*, Intel i8255x, Realtek 8120/8139, NE2000, SiS 900) should also work. No other network expansion boards (ATM, FDDI, Gigabit Ethernet) are supported.

Realtek RTL8150L USB-based Ethernet-adapters on one of the supported USB-controllers are supported.

Storage

Storage-I/O is at the moment supported via either the NCR 53C700 narrow, NCR 53C710 Fast-Narrow or the NCR 53C875 Ultra-Wide SE SCSI-controllers available in some of these machines. The on-board NCR 53C720 Fast-Wide HVD controllers are not supported. GSC/HSC and PCI-expansion cards with one of the 53C710 or 53C8xx (siop) SCSI-chipsets, Adaptec 2940 (ahc) PCI and certain Qlogic ISP PCI SCSI adapters should also work, however not necessarily for booting.

Graphics

All on-board graphics adapters are supported for text-mode via STI-routines (similar to PC VGA BIOS). At the present, there is no working X-server, so there are no graphics capabilities for now.

Human-I/O

Human-I/O is supported via PS/2 devices, HIL does not work.

Misc

Several PCI USB-Adapters from VIA and ALi have been tested and are known to work; they support USB mass-storage devices (ie flash-based and harddrives).

3.3.4 References

- **NetBSD/hp700**[35] is the official page of the port.
- From **ftp.netbsd.org**[36] and its mirrors you can download complete binary snapshots of the NetBSD/hp700-port (check for the dates). The **INSTALL.html**[37] document contains instructions for installation.

[35] http://www.netbsd.org/Ports/hp700/
[36] ftp://ftp.netbsd.org/pub/NetBSD/arch/hp700/snapshot/
[37] ftp://ftp.netbsd.org/pub/NetBSD/arch/hp700/snapshot/20050501-3.99.3/INSTALL.html

3.4 NeXTSTEP/hppa

3.4.1 Overview

NeXTSTEP was introduced in 1989 as an UNIX implementation by NeXT. NeXTSTEP features a complete development and user environment, an unique GUI, a special display system, the DPS (*Display Post Script*). The underlying core is a *MACH* microkernel, 4.3BSD compatible and extensible at runtime. At the time of its introduction 1989, NeXTSTEP v0.8 only ran on the so called *black hardware*, rather expensive m68k-systems also produced by NeXT. In 1991 Version 3.1 was introduced and for the first time *white hardware* (x86) was supported. The development line (m68k and x86) was continued and around 1994 Version 3.3 with support for certain RISC-computers was released, including some Sun SPARC and HP PA-RISC 1.1 systems.

The 715/100XC workstation is probably the fastest non-white (i.e. not Intel-based) workstation compatible with the original NeXTSTEP.

3.4.2 Supported Systems

NeXTSTEP runs only on several older PA-RISC workstation models based on either a PA-7100 or PA-7100LC CPU and the ASP or LASI chipset.

- 712/{60,80,100}
- 715/{33,50,75}
- 715/{64,80,100,100XC}
- 725/{50,64,75,100}
- 735/{99,125}
- 755/{99,125}

3.4.3 Supported Hardware

- It needs for a normal user-environment about 400MB of harddisk; complete user and developer environment should take about 700MB
- 32MB of RAM should be sufficient, 64MB are better
- Not more than 256MB RAM is supported
- All onboard graphics-adaptors and the CRX, CRX-24 adaptors are supported. HCRX and HCRX-24 (Hyperdrive) adaptors are only supported after installing the NeXTSTEP 3.3 patches (see below in *References* for the link)
- On 712 and 715/{64,80,100} you have to use the PS/2 keyboards, HIL will not work on these systems, on the other systems HIL is supported
- **Not supported** are notably on the 735/755 the FWD (Fast/Wide Differential) SCSI subsystem and the optional FDDI network boards

3.4.4 Installation

You'll need a CD-ROM drive that supports a blocksize of 512 Bytes (Plextor, HP, some Toshiba) to install NeXTSTEP. Put this on your PA-RISC box and set the SCSI-ID to `1`. If your CD-ROM has an higher ID than `1` you could get annoying read-errors while reading. Your harddisk should be at ID `0` when performing the install.

Important to note is that the harddrive you want to install NeXTSTEP on should not be larger than 4GB, otherwise the installation could get tricky. Moreover, it is recommended to completely wipe the harddrive of any existing filesystems before starting the installation.

Now power up the box and hold down `<ESC>` while booting. In the PDC boot the NeXTSTEP installation CD by typing `boot scsi.1`. Follow the instructions for installing NeXTSTEP and then sit back and relax. When the installation is finished I'd recommend to configure your boot-drive with the SCSI-ID `5` and the CD-ROM at ID `4` since the PDC boot-loader begins its search for an operating system from the highest SCSI-ID.

3.4.5 References

- **The NEXTSTEP/OpenStep FAQ**[38] Extensive collection of information on topics surrounding NeXTSTEP software and hardware support. Bernhard Scholz (2000?). [Mirrored at channelu.com, original peanuts.org unavailable]
- **NeXTstep 3.3 Network and System Administration Manual**[39] Information on configuration of network services, user management, storage, directory services and more. NeXT Software Inc. (1994). [Converted HTML version: Randall J. Rencsok (2000: channelu.com)]
- **NeXTstep 3.3 Developer Documentation Manuals**[40] Documentation for the integrated development tools in NeXTstep and the several APIs and frameworks. NeXT Software Inc. (1994). [Converted HTML version: Randall J. Rencsok (2000: channelu.com)]

There used to be a large software archive available at the Peanuts.org FTP server. It sadly is gone, and there is apparently no complete mirror of it.

[38] http://www.channelu.com/NeXT/NeXTFAQ-new/NeXTFAQ.toc.html
[39] http://www.channelu.com/NeXT/NeXTStep/3.3/nsa/index.html
[40] http://www.channelu.com/NeXT/NeXTStep/3.3/nd/index.html

3.5 OpenBSD/hppa

3.5.1 Overview

Work on an OpenBSD port to PA-RISC HP 9000/700 systems started around 1999. Main sources of information and code at that time were mainly the previous porting efforts Lites/HPPA and MkLinux.

The **OpenBSD/hppa** port focuses on **32-bit** PA-RISC 1.x computers (based on PA-7100, PA-7100LC, PA-7200 and PA-7300LC CPUs) and some of the 64-bit models running in 32-bit mode (based on PA-8000, PA-8200 and PA-8500).

OpenBSD/hppa is since version 3.5 a full featured release, albeit still with limitations, as there is no working X-server and still many unsupported machines and I/O-devices. At the current state, it is possible to boot OpenBSD/hppa on all supported systems either from the network or from SCSI drives, though not all SCSI controllers are supported (see below).

NetBSD/hp700 is heavily based on this OpenBSD/hppa port.

The **OpenBSD/hppa64** port to support PA-RISC 2.0 computers running in full **64-bit** mode is in its beginning stages.

3.5.2 Supported 32-bit Systems

Systems supported by the **32-bit** OpenBSD/hppa port.

- 712/{60,80,100}
- 715/{33,50,75}, 715/{64,80,100}
- 725/{50,75,100}
- 735/{99,125}
- 742i/50
- 743i/{64,100}
- 744/{132L,165L}
- 745i/{50,100}
- 745/{132L,165L}
- 747i/{50,100}
- 748i/{64,100}, 748/{132L,165L}
- 755/{99,125}
- A180[C]
- B132L, B160L, B132L+, B180L+
- J200, J210[XC]
- C100, C110, C132L, C160L, C160, C180 *(See Note 1)*, C200, C240, C360 *(See Note 1)*
- D220, D230, D320, D330
- RDI PrecisionBook
- SAIC Galaxy 1100

Notes

1. Running the system in 32-bit mode

3.5.3 Supported hardware

Buses and Chipsets

All PCI and GSC buses and onboard bus-controllers (ASP, LASI, Dino/Cujo, U2/Uturn) on the above machines are supported. Additionally, Yenta-compatible PCI-Cardbus bridges are supported, as e.g. found on the RDI Precisionbook.

The ISA/EISA and HP-PB buses and bus-controllers are not supported. Support for the EISA bus-controller is in the works.

Networking

All on-board Ethernet and Fast-Ethernet network interfaces on any of the above machines are supported; the FDDI-sliders on the 735/755 are not supported. Expansion cards for the GSC/HSC and PCI-bus slots with a supported Ethernet chipset (Intel i82596, DEC 21142/43 *Tulip*, Intel EtherExpress PRO/10 and PRO/100 series in various incarnations for the PCI bus, NE2000-compatible) should also work. PCMCIA (and to a lesser extent Cardbus) devices are supported in a compatible PCI-Cardbus bridges, including IEEE802.11b WLAN adapters and Ethernet cards. No other network expansion boards (ATM, FDDI, Gigabit-Ethernet) are supported.

Storage

Storage-I/O is at the moment supported via either the NCR 53C700 narrow, NCR 53C710 Fast-Narrow or the NCR 53C875 Ultra-Wide SE SCSI-controllers available in some of these machines. The on-board NCR 53C720 Fast-Wide HVD controllers are *not* supported. GSC/HSC and PCI-expansion cards with one of the 53C710 or 53C8xx SCSI-chipsets and Adaptec 2940 PCI SCSI adapters should also work, though are not neccessarily bootable.

Graphics

All on-board graphics adapters are supported for text-mode via STI-routines (similar to PC VGA BIOS), additionally the CRX, CRX-24, HCRX-8, HCRX-24 graphics expansion boards (GSC) are supported. At the present, there is no working X-server for OpenBSD/hppa, so there are no graphics (X11) capabilities for now.

Human-I/O

Human-I/O is supported via either the PS/2 or HIL on-board interfaces, though not all HIL-devices are supported.

3.5.4 Software

- Lots of binaries of popular open source programs are available for the 32-bit OpenBSD/hppa port through the **OpenBSD Packages system**[41].
- **OpenBSD: Getting Packages**[42] describes the required steps to fetch and install these packages.
- An even larger array of software can be obtained through the use of the **OpenBSD Ports tree**[43], which provides a framework for automatic compiling popular opensource software.

3.5.5 References

- **OpenBSD/hppa**[44] Official page of the 32-bit PA-RISC port of OpenBSD. The OpenBSD Project (November 2005). Accessed 12 Dec 2005.
- **Snapshots directory at ftp.openbsd.org**[45] Contains complete binary snapshots (which are easily installable) of 32-bit OpenBSD/hppa. The OpenBSD Project (November/December 2005). Accessed 12 Dec 2005.
- **INSTALL.hppa**[46] in the Snapshots directory Extensive installation instructions for the snapshots. The OpenBSD Project (December 2005). Accessed 12 Dec 2005.
- **OpenBSD/hppa64**[47] Official page of the 64-bit PA-RISC port of OpenBSD. The OpenBSD Project (May 2005). Accessed 12 Dec 2005.

[41] ftp://ftp.openbsd.org/pub/OpenBSD/snapshots/packages/hppa/
[42] http://www.openbsd.org/ports.html#Get
[43] http://www.openbsd.org/ports.html#Use
[44] http://www.openbsd.org/hppa.html
[45] ftp://ftp.openbsd.org/pub/OpenBSD/snapshots/hppa/
[46] ftp://ftp.openbsd.org/pub/OpenBSD/snapshots/hppa/INSTALL.hppa
[47] http://www.openbsd.org/hppa64.html

3.6 Other PA-RISC Operating Systems

3.6.1 Overview

Several other operating systems have been ported to the PA-RISC over the time. Most of them only reached development state and have long been not maintained anymore. Documentation is rare and getting sources and/or distributions is even harder.

3.6.2 MkLinux

Overview

The first MkLinux for PA-RISC Snapshots were published by OSF/The Open Group, which in this form no longer exist today. They took the Mach/hppa kernel sources from the Utah University and improved the kernel and put a Linux (2.0.32) server ("personality") on it. The result was called *Open Group RI Microkernel (pmk1.1)*. Included in the Open Group distribution were X11R6 patches, the GNU ELF-compiler and debugger and complete `/usr` and `/var` directories.

MkLinux was the first free operating system that truly *ran* on PA-RISC hardware (in contrast to Mach, which suffered from unfinished development and a lot of bugs on PA-RISC). However, the system was quite sluggish (with some blaming it on the underlying Mach microkernel), software support was quite crude and at the time of its active development PA-RISC workstations were not really largely distributed to private end-users (i.e., there wasn't the large hobbyist userbase PA-RISC has now).

Its use is not encouraged anymore.

Supported Hardware

- 705, 710, 720, 730, 750 (based on PA-7000 processors)
- 715/{33,50,75}, 725/{50,75}, 735/{99,125}, 755/{99,125} (based on PA-7100 processors)
- 712/{60,80,100}, 715/{64,80,100}, 725/100 (based on PA-7100LC processors)
- C100, C110 (based on PA-7200 processors)
- SCSI (internal single-ended, internal fast-wide-differential, GSC-based fast-wide-differential, and EISA fast-differential), RS232 serial, builtin Ethernet, Video (GRX, CRX and Artist), HIL and PS/2, audio

References

- **ftp://ftp.cirr.com/pub/hppa/mklinux**[48] Mirror of the MkLinux sets at ftp.cirr.com
- **Release Notes for MkLinux on HP PA-RISC**[49] Descriptions on MkLinux and extensive installation instructions. The Open Group (1997), and the Central Iowa (Model) Railroad (1999) [mirror]. Accessed 05 Oct 2005.

[48] ftp://ftp.cirr.com/pub/hppa/mklinux/
[49] ftp://ftp.cirr.com/pub/hppa/mklinux/mkpa-rel.html

3.6.3 HPBSD

Overview

Mike Hibler's HPBSD was the first non-commercial OS for the PA-RISC platform. Developed at the University of Utah, it grew out of a port of 4.3BSD to the m68k-based HP 9000/300 and 400 systems. Due to the pollution of the code with HP HP-UX and AT&T distribution was confined to a small circle of entities with the required appropriate source licences (and as such generally not available to the broaded hobbyist public). Active work mainly happened during the early and mid-90s, with only small fixes commited afterwards.

Supported Hardware

- 705, 710, 720, 730, 750 (based on PA-7000 processors)
- 715/{33,50,75}, 725/{50,75}, 735/{99,125}, 755/{99,125} (based on PA-7100 processors)
- 712/{60,80,100}, 715/{64,80,100}, 725/100 (based on PA-7100LC processors)
- J200, J210[XC], C100, C110 (based on PA-7200 processors)
- SCSI (internal single-ended, internal fast-wide-differential, GSC based fast-wide-differential, and EISA fast-differential), RS232 serial, builtin Ethernet, Video (GRX, CRX and Artist), HIL and PS/2, audio

History

(*Taken with permission from Mike Hibler (1999)*)

HPBSD for m68k-based systems was born in 1987 when Mike Hibler started a port of 4.3BSD to the HP 9000/320 and 350 workstations at the University of Utah. Major development lasted until about 1991 with the final addition of Motorola 68040 support.

Sometime in the fall of 1989, Jeff Forys started work on the hp800 (PA-RISC) port starting with a hybrid HP-UX/Mach kernel called *Tut* that was done as an experiment at HP Labs. By around February 1990 HPBSD was limping along on an 9000/835 and by later that year was running solidly on the PA.

For a short period of time in 1989-90, Mt Xinu also worked on the PA-RISC port. They actually produced the first usable part of the port, the boot loader, late in 1989. HPBSD used (and continues to use) this boot loader.

In 1990, yet another Mach project was spun off of HPBSD. This was a Mach 3.0 + UX single server port for the 835 sponsored by HP and done primarily by Bob Wheeler. Around 1992, this port mutated into a Mach 3.0 + OSF/1 single server port for the 700 series (800 was dropped) and eventually became the Mach4 + Lites system available to the public (see Mach4/Lites entry).

Starting in May 1991, Leigh Stoller ported HPBSD to the HP 9000/720 workstation. In January 1992, the hp300 and hp800 kernels were merged into a common source tree.

The last major development to HPBSD was the addition of the 4.4BSD kernel filesystem and networking code and the 4.4BSD ANSI-compliant C library. Jeff Forys started this in April 1992 and by early 1993 all of the University of Utah's HPBSD machines had been converted. This version was known as HPBSD 2.0. Since this merge included the NFS implementation done by Rick Macklem, all

Sun encumbered code could be eliminated. In April 1993, a semi-formal release of HPBSD 2.0 was made to the 2-3 sites which had the necessary agreements with HP (necessary to obtain the PA-RISC specific code). Since that time, active development of HPBSD had pretty much stopped.

As of Summer 1999, there were less than ten HPBSD machines left: one 68k and the rest PA-RISC. The last significant efforts were to bring HP-UX compatibility up to 10.20 (to run the JDK) and to port a 3Com EISA 100Mbit ethernet driver.

References

- **HPBSD: Utah's 4.3bsd port for HP9000 series machines**[50] Original homepage of the HPBSD project. Mike Hibler (July 1999: University of Utah). Accessed 04 Oct 2005.

3.6.4 Mach4/Lites

The Utah University ported the original Mach microkernel with a 4.4BSD-Lites server on it to the PA-RISC architecture. *'We refer to this as a snapshot and not a release as the provided code is not robust, does not provide a complete application environment, contains minimal bootstrap capability, and has practically no documentation. Hence, we recommend that you do not run this, unless you are a hard-core O.S. hacker who has an interest in, and knowledge of, the PA architecture. Later true releases, with help from you O.S. hackers, will allow the more faint-at-heart to run an alternative O.S. on their HP workstations.'*

3.6.5 Chorus

Overview

Chorus was like Mach a micro-kernel based operating system.

Citing a mail from Jon Inouye from December 1st, 1994, regarding the history of the PA-RISC port of the CHORUS OS:

```
Prof. Jonathan Walpole supervised a port of the CHORUS v3.3
nucleus to the Hewlett-Packard 9000/834 workstation from late
1990 to mid-1991. This was part of a funded research project
to evaluate the CHORUS operating system with respect to the
Hewlett-Packard PA-RISC architecture. The nucleus did not
support any disk/network drivers and performed all console/
keyboard I/O though IODC (PROM) routines. A CHORUS/MiX V.3.2
Process Manager (PM) port was partially completed to the point
where UNIX shells and certain system calls were supported ...
but not a UNIX file system.

Since then, I have been porting Chorus/MiX V.3.2 (with the v3.4
nucleus) to the HP 9000/720. Since I am performing this port in
```

[50] http://www.cs.utah.edu/~mike/hpbsd/hpbsd.html

my spare time it is not progressing very fast. The v3.4 nucleus runs along with a serial driver. It lacks other device drivers, FP emulation support (though basic FP operations are supported) and still uses the old HP-UX PDIR structure rather than the more recent HPT. The Ethernet driver is still being debugged as is an ancient version of the MiX V.3.2 PM. The port is being used for virtual memory experiments.

Both ports use a considerable amount (over 40,000 lines combined) of HP-UX source code for the assembly language utilities, boot up, I/O initialization, and device drivers. The 834 port uses a Tut (HP-UX 2.0 modified to run Mach 2.0) base and the 720 port uses a HP-UX 8.0 base. For this reason, we have not been able to release anything because of all the legal implications ... HP, Chorus, USL copyrights.

Chapter 4

PA-RISC Computer Systems

4.1 PA-RISC Computers

This page lists the various PA-RISC based HP 9000 computers, sorted into tables according to the type of their case and general classification. Detailed, separate pages with more in-depth specifications are available for most systems. Results from the SPEC suite of benchmarks are collected on a separate benchmarks page.

HP produced also a line of RISC-based (though not PA-RISC) X-Terminals, often sold with HP 9000 workstations. The x-terminals page describes those.

A separate page exists for the HP 9000/520 workstations, one of the predecessors of the PA-RISC systems and HP's first Unix workstations.

4.1.1 Pizzabox

These are really small, pizza-box sized desktop computers. They easily fit as a monitor stand.

Model	CPU	I/D cache per CPU	max. RAM	Expansion	OS
705	PA-7000 35MHz	32/64KB	128MB	0	HP-UX (up to 11.00 *(See Note 1)*), Linux
710	PA-7000 50MHz	32/64KB	128MB	0	HP-UX (up to 11.00 *(See Note 1)*), Linux
712/60	PA-7100LC 60MHz	64KB	128MB	1 GIO 1 TSIO	HP-UX (up to 11i), Linux, NetBSD, NeXTSTEP, OpenBSD
712/80	PA-7100LC 80MHz	256KB	128MB	1 GIO 1 TSIO	HP-UX (up to 11i), Linux, NetBSD, NeXTSTEP, OpenBSD
712/100	PA-7100LC 100MHz	256KB	192MB	1 GIO 1 TSIO	HP-UX (up to 11i), Linux, NetBSD, NeXTSTEP, OpenBSD

Notes

1. HP-UX 10.20 is the last officially supported version, certain releases of 11.0 and 11i (11.11) might also work. The denoted version is the last release known to work.

4.1.2 Portable/Laptop

There also were PA-RISC computers which featured an integrated keyboard and LCD and could be carried around more or less easily.

Model	CPU	I/D cache per CPU	max. RAM	Expansion	OS
PrecisionBook 132 *(RDI)*	PA-7300LC 132MHz	64/64KB (+ 1MB)	512MB	2 Cardbus	HP-UX (up to 11i), Linux, NetBSD, OpenBSD
PrecisionBook 160 *(RDI)*	PA-7300LC 160MHz	64/64KB (+ 1MB)	512MB	2 Cardbus	HP-UX (up to 11i), Linux, NetBSD, OpenBSD
PrecisionBook 180 *(RDI)*	PA-7300LC 180MHz	64/64KB (+ 1MB)	512MB	2 Cardbus	HP-UX (up to 11i), Linux, NetBSD, OpenBSD
Galaxy 1100 *(SAIC)*	PA-7100LC 60MHz	64KB	128MB	2 PCMCIA	HP-UX (up to 11i), Linux, NetBSD, OpenBSD
Galaxy 1100 *(SAIC)*	PA-7100LC 80MHz	256KB	128MB	2 PCMCIA	HP-UX (up to 11i), Linux, NetBSD, OpenBSD

4.1.3 Desktop

PA-RISC computers were available in several different desktop formats, ranging from rather small desktops (715, B-Class) to wide and heavy cases, which barely fit on a normal desk (730/735, C-Class).

Model	CPU	I/D cache per CPU	max. RAM	Expansion	OS
715/33	PA-7100 33MHz	64/64KB	192MB	1 EISA/SGC	HP-UX (up to 11.00 *(See Note 1)*), Linux, NetBSD, NeXTSTEP, OpenBSD
715/50	PA-7100 50MHz	64/64KB	256MB	1 EISA/SGC	HP-UX (up to 11.00 *(See Note 1)*), Linux, NetBSD, NeXTSTEP, OpenBSD
715/64	PA-7100LC 64MHz	256KB	256MB	1 EISA/GSC	HP-UX (up to 11i), Linux, NetBSD, NeXTSTEP, OpenBSD

715/75	PA-7100 75MHz	256/256KB	256MB	1 EISA/SGC	HP-UX (up to 11.00 *(See Note 1)*), Linux, NetBSD, NeXTSTEP, OpenBSD
715/80	PA-7100LC 80MHz	256KB	256MB	1 EISA/GSC	HP-UX (up to 11i), Linux, NetBSD, NeXTSTEP, OpenBSD
715/100	PA-7100LC 100MHz	256KB	256MB	1 EISA/GSC	HP-UX (up to 11i), Linux, NetBSD, NeXTSTEP, OpenBSD
715/100XC	PA-7100LC 100MHz	1MB	256MB	1 EISA/GSC	HP-UX (up to 11i), Linux, NetBSD, NeXTSTEP, OpenBSD
720	PA-7000 50MHz	128/256KB	?	1 EISA 1 SGC	HP-UX (up to 10.20), Linux
725/50	PA-7100 50MHz	64/64KB	256MB	3 EISA 1 EISA/SGC	HP-UX (up to 11.00 *(See Note 1)*), Linux, NetBSD, NeXTSTEP, OpenBSD
725/75	PA-7100 75MHz	256/256KB	256MB	3 EISA 1 EISA/SGC	HP-UX (up to 11.00 *(See Note 1)*), Linux, NetBSD, NeXTSTEP, OpenBSD
725/100	PA-7100LC 100MHz	256KB	256MB	1 EISA 3 EISA/GSC	HP-UX (up to 11i), Linux, NetBSD, NeXTSTEP, OpenBSD
730	PA-7000 66MHz	128/256KB	?	1 EISA 1 SGC	HP-UX (up to 10.20), Linux
735/99	PA-7100 99MHz	256/256KB	784MB	1 EISA 1 SGC	HP-UX (up to 11i *(See Note 1)*), Linux, NetBSD, NeXTSTEP, OpenBSD

735/125	PA-7150 125MHz	256/256KB	784MB	1 EISA 1 SGC	HP-UX (up to 11i *(See Note 1)*), Linux, NetBSD, NeXTSTEP, OpenBSD
B132L	PA-7300LC 132MHz	64/64KB (+ 1MB)	1.5GB	1 GSC/PCI 1 GSC/PCI/EISA	HP-UX (up to 11i), Linux, NetBSD, OpenBSD
B132L+	PA-7300LC 132MHz	64/64KB (+ 1MB)	1.5GB	1 GSC/PCI 1 GSC/PCI/EISA	HP-UX (up to 11i), Linux, NetBSD, OpenBSD
B160L	PA-7300LC 160MHz	64/64KB (+ 1MB)	1.5GB	1 GSC/PCI 1 GSC/PCI/EISA	HP-UX (up to 11i), Linux, NetBSD, OpenBSD
B180L+	PA-7300LC 180MHz	64/64KB (+ 1MB)	1.5GB	1 GSC/PCI 1 GSC/PCI/EISA	HP-UX (up to 11i), Linux, NetBSD, OpenBSD
B2600	PA-8600 500MHz	0.5/1MB	4GB	4 PCI	HP-UX (up to 11i), Linux
C100	PA-7200 100MHz	256/256KB	1GB	1 GSC 3 EISA/GSC	HP-UX (up to 11i), Linux, OpenBSD
C110	PA-7200 120MHz	256/256KB	1GB	1 GSC 3 EISA/GSC	HP-UX (up to 11i), Linux, OpenBSD
C132L	PA-7300LC 132MHz	64/64KB (+ 1MB)	2GB	1 GSC/PCI 1 GSC/PCI/EISA 2 GSC/EISA	HP-UX (up to 11i), Linux, NetBSD, OpenBSD
C160L	PA-7300LC 160MHz	64/64KB (+ 1MB)	2GB	1 GSC/PCI 1 GSC/PCI/EISA 2 GSC/EISA	HP-UX (up to 11i), Linux, NetBSD, OpenBSD
C160	PA-8000 160MHz	512/512KB	3GB	1 GSC/PCI 1 GSC/PCI/EISA 2 GSC/EISA	HP-UX (up to 11i), Linux, OpenBSD
C180	PA-8000 180MHz	1/1MB	3GB	1 GSC/PCI 1 GSC/PCI/EISA 2 GSC/EISA	HP-UX (up to 11i), Linux, OpenBSD
C200	PA-8200 200MHz	0.5/1MB	3GB	3 GSC/PCI 1 GSC/PCI/(EISA)	HP-UX (up to 11i), Linux, OpenBSD
C240	PA-8200 236MHz	2/2MB	3GB	3 GSC/PCI 1 GSC/PCI/(EISA)	HP-UX (up to 11i), Linux, OpenBSD

C360	PA-8500 367MHz	0.5/1MB	3GB	3 GSC/PCI 1 GSC/PCI/(EISA)	HP-UX (up to 11i), Linux, OpenBSD

Notes

1. HP-UX 10.20 is the last officially supported version, certain releases of 11.00 and 11i (11.11) might also work. The denoted version is the last release known to work.

4.1.4 Mini-Tower

Some PA-RISC computers were delivered in a minitower case, which fits easily below the desk. The newer workstations (with four digits) feature a black PC-like case while the older J-Class systems are build into a very heavy, beige minitower.

Model	CPU	I/D cache per CPU	max. RAM	Expansion	OS
B1000	PA-8500 300MHz	0.5/1MB	8GB	6 PCI	HP-UX (up to 11i), Linux
B2000	PA-8500 400MHz	0.5/1MB	4GB	4 PCI	HP-UX (up to 11i), Linux
C3000	PA-8500 400MHz	0.5/1MB	8GB	6 PCI	HP-UX (up to 11i), Linux
C3600	PA-8600 552MHz	0.5/1MB	8GB	6 PCI	HP-UX (up to 11i), Linux
C3650	PA-8700 625MHz	0.75/1.5MB	8GB	6 PCI	HP-UX (up to 11i), Linux
C3700	PA-8700 750MHz	0.75/1.5MB	8GB	6 PCI	HP-UX (up to 11i), Linux
C3750	PA-8700+ 875MHz	0.75/1.5MB	8GB	6 PCI	HP-UX (up to 11i), Linux
C8000	2 PA-8800/PA-8900 900MHz/1GHz/1.1GHz	1.5/1.5MB + 32MB/64MB	32GB	6 PCI 1 AGP8X	HP-UX (11i)
J200	1-2 PA-7200 100MHz	256/256KB	2GB	1 GSC 2 EISA 2 GSC/EISA	HP-UX (up to 11i), Linux, OpenBSD
J210	1-2 PA-7200 120MHz	256/256KB	2GB	1 GSC 2 EISA 2 GSC/EISA	HP-UX (up to 11i), Linux, OpenBSD
J210XC	1-2 PA-7200 120MHz	1/1MB	2GB	1 GSC 2 EISA 2 GSC/EISA	HP-UX (up to 11i), Linux, OpenBSD
J280	PA-8000 180MHz	1/1MB	2GB	1 GSC 2 EISA 2 GSC/EISA	HP-UX (up to 11i), Linux
J282	1-2 PA-8000 180MHz	1/1MB	2GB	1 GSC 2 EISA 2 GSC/EISA	HP-UX (up to 11i), Linux
J2240	1-2 PA-8200 236MHz	2/2MB	4GB	1 PCI 1 PCI/EISA 3 GSC/PCI	HP-UX (up to 11i), Linux

J5000	1-2 PA-8500 440MHz	0.5/1MB	8GB	7 PCI	HP-UX (up to 11i), Linux
J5600	1-2 PA-8600 552MHz	0.5/1MB	8GB	7 PCI	HP-UX (up to 11i), Linux
J6000	1-2 PA-8600 552MHz	0.5/1MB	16GB	3 PCI	HP-UX (up to 11i), Linux
J6700	1-2 PA-8700 750MHz	0.75/1.5MB	16GB	3 PCI	HP-UX (up to 11i), Linux
J6750	1-2 PA-8700+ 875MHz	0.75/1.5MB	16GB	3 PCI	HP-UX (up to 11i), Linux
J7000	1-4 PA-8500 440MHz	0.5/1MB	16GB	7 PCI	HP-UX (up to 11i), Linux
J7600	1-4 PA-8600 552MHz	0.5/1MB	16GB	7 PCI	HP-UX (up to 11i), Linux

4.1.5 Tower/Deskside

This class of systems spans mostly server systems which are big and bulky and very noisy. Their cases vary greatly, from smaller towers (D-Class/E-Class) up to rack-mountable deskside systems (K-Class).

Model	**CPU**	**I/D cache per CPU**	**max. RAM**	**Expansion**	**OS**
750	PA-7000 66MHz	256/256KB	?	4 EISA 2 SGC	HP-UX (up to 10.20), Linux
755/99	PA-7100 99MHz	256/256KB	768MB	4 EISA 2 SGC	HP-UX (up to 11i *(See Note 1)*), Linux, NetBSD, NeXTSTEP, OpenBSD
755/125	PA-7150 125MHz	256/256KB	768MB	4 EISA 2 SGC	HP-UX (up to 11i *(See Note 1)*), Linux, NetBSD, NeXTSTEP, OpenBSD
D200	PA-7100LC 75MHz	256KB	512MB	2 EISA 1 GSC 3 EISA/GSC	HP-UX (up to 11i), Linux
D210	PA-7100LC 100MHz	256KB	512MB	2 EISA 1 GSC 3 EISA/GSC	HP-UX (up to 11i), Linux
D220	PA-7300LC 132MHz	64/64KB (+ 1MB)	1GB	2 EISA 1 GSC 3 EISA/GSC	HP-UX (up to 11i), Linux, OpenBSD
D230	PA-7300LC 160MHz	64/64KB (+ 1MB)	1GB	2 EISA 1 GSC 3 EISA/GSC	HP-UX (up to 11i), Linux, OpenBSD
D250	1-2 PA-7200 100MHz	256/256KB	1.5GB	2 EISA 1 GSC 3 EISA/GSC	HP-UX (up to 11i), Linux
D260	2 PA-7200 120MHz	1/1MB	1.5GB	2 EISA 1 GSC 3 EISA/GSC	HP-UX (up to 11i), Linux
D270	1-2 PA-8000 160MHz	512/512KB	3GB	2 EISA 1 GSC 3 EISA/GSC	HP-UX (up to 11i), Linux

D280	1-2 PA-8000 180MHz	1/1MB	3GB	2 EISA 1 GSC 3 EISA/GSC	HP-UX (up to 11i), Linux
D300	PA-7100LC 75MHz	256KB	512MB	3 EISA 1 GSC 4 EISA/GSC	HP-UX (up to 11i), Linux
D310	PA-7100LC 100MHz	256KB	512MB	3 EISA 1 GSC 4 EISA/GSC	HP-UX (up to 11i), Linux
D320	PA-7300LC 132MHz	64/64KB (+ 1MB)	1GB	3 EISA 1 GSC 4 EISA/GSC	HP-UX (up to 11i), Linux, OpenBSD
D330	PA-7300LC 160MHz	64/64KB (+ 1MB)	1GB	3 EISA 1 GSC 4 EISA/GSC	HP-UX (up to 11i), Linux, OpenBSD
D350	1-2 PA-7200 100MHz	256/256KB	1.5GB	3 EISA 1 GSC 4 EISA/GSC	HP-UX (up to 11i), Linux
D360	2 PA-7200 120MHz	1/1MB	1.5GB	3 EISA 1 GSC 4 EISA/GSC	HP-UX (up to 11i), Linux
D370	1-2 PA-8000 160MHz	512/512KB	3GB	3 EISA 1 GSC 4 EISA/GSC	HP-UX (up to 11i), Linux
D380	1-2 PA-8000 180MHz	1/1MB	3GB	3 EISA 1 GSC 4 EISA/GSC	HP-UX (up to 11i), Linux
D390	1-2 PA-8200 240MHz	2/2MB	3GB	3 EISA 1 GSC 4 EISA/GSC	HP-UX (up to 11i), Linux
E25	PA-7100LC 48MHz	64KB	512MB	2-4 HP-PB	HP-UX (up to 11i *(See Note 2)*), Linux, NetBSD
E35	PA-7100LC 64MHz	256KB	512MB	2-4 HP-PB	HP-UX (up to 11i *(See Note 2)*), Linux, NetBSD
E45	PA-7100LC 80MHz	256KB	512MB	2-4 HP-PB	HP-UX (up to 11i *(See Note 2)*), Linux, NetBSD
E55	PA-7100LC 96MHz	1MB	512MB	2-4 HP-PB	HP-UX (up to 11i *(See Note 2)*), Linux, NetBSD
F10	PA-7000 32MHz	32/64KB	768MB	2? HP-PB	HP-UX (up to 11i *(See Note 2)*)
F20	PA-7000 48MHz	64/64KB	768MB	2? HP-PB	HP-UX (up to 11i *(See Note 2)*)
F30	PA-7000 48MHz	256/256KB	768MB	2? HP-PB	HP-UX (up to 11i *(See Note 2)*)
G30	PA-7000 48MHz	256/256KB	768MB	4 HP-PB	HP-UX (up to 11i *(See Note 2)*)
G40	PA-7100 64MHz	256/256KB	768MB	4 HP-PB	HP-UX (up to 11i *(See Note 2)*)
G50	PA-7100 96MHz	256/256KB	768MB	4 HP-PB	HP-UX (up to 11i *(See Note 2)*)
G60	PA-7100 96MHz	1/1MB	768MB	4 HP-PB	HP-UX (up to 11i *(See Note 2)*)
G70	1-2 PA-7100 96MHz	2/2MB	768MB	4 HP-PB	HP-UX (up to 11i *(See Note 2)*)

H20	1 PA-7000 48MHz	64/64KB	768MB	8 HP-PB	HP-UX (up to 11i *(See Note 2)*)
H30	PA-7000 48MHz	256/256KB	768MB	8 HP-PB	HP-UX (up to 11i *(See Note 2)*)
H40	PA-7100 64MHz	256/256KB	768MB	8 HP-PB	HP-UX (up to 11i *(See Note 2)*)
H50	PA-7100 96MHz	256/256KB	768MB	8 HP-PB	HP-UX (up to 11i *(See Note 2)*)
H60	PA-7100 96MHz	1/1MB	768MB	8 HP-PB	HP-UX (up to 11i *(See Note 2)*)
H70	1-2 PA-7100 96MHz	2/2MB	768MB	8 HP-PB	HP-UX (up to 11i *(See Note 2)*)
I30	PA-7000 48MHz	256/256KB	768MB	12 HP-PB	HP-UX (up to 11i *(See Note 2)*)
I40	PA-7100 64MHz	256/256KB	768MB	12 HP-PB	HP-UX (up to 11i *(See Note 2)*)
I50	PA-7100 96MHz	256/256KB	768MB	12 HP-PB	HP-UX (up to 11i *(See Note 2)*)
I60	PA-7100 96MHz	1/1MB	768MB	12 HP-PB	HP-UX (up to 11i *(See Note 2)*)
I70	1-2 PA-7100 96MHz	2/2MB	768MB	12 HP-PB	HP-UX (up to 11i *(See Note 2)*)
K100	PA-7200 100MHz	256/256KB	512MB	1 HSC 4 HP-PB	HP-UX (up to 11i), Linux
K200	1-4 PA-7200 100MHz	256/256KB	4GB	1 HSC 4 HP-PB	HP-UX (up to 11i), Linux
K210	1-4 PA-7200 120MHz	256/256KB	4GB	1 HSC 4 HP-PB	HP-UX (up to 11i), Linux
K220	1-4 PA-7200 120MHz	1/1MB	4GB	1 HSC 4 HP-PB	HP-UX (up to 11i), Linux
K250	1-4 PA-8000 160MHz	1/1MB	4GB	1 HSC 4 HP-PB	HP-UX (up to 11i), Linux
K260	1-4 PA-8000 180MHz	1/1MB	4GB	1 HSC 4 HP-PB	HP-UX (up to 11i), Linux
K370	1-6 PA-8200 200MHz	2/2MB	4GB	3 HSC 4 HP-PB	HP-UX (up to 11i), Linux
K380	1-6 PA-8200 240MHz	2/2MB	4GB	3 HSC 4 HP-PB	HP-UX (up to 11i), Linux
K400	1-4 PA-7200 100MHz	256/256KB	2GB	1-5 HSC 8 HP-PB	HP-UX (up to 11i), Linux
K410	1-4 PA-7200 120MHz	256/256KB	2GB	1-5 HSC 8 HP-PB	HP-UX (up to 11i), Linux
K420	1-4 PA-7200 120MHz	1/1MB	8GB	1-5 HSC 8 HP-PB	HP-UX (up to 11i), Linux
K450	1-4 PA-8000 160MHz	1/1MB	8GB	1-5 HSC 8 HP-PB	HP-UX (up to 11i), Linux
K460	1-4 PA-8000 180MHz	1/1MB	8GB	1-5 HSC 8 HP-PB	HP-UX (up to 11i), Linux
K570	1-6 PA-8200 200MHz	2/2MB	8GB	9 HSC 4 HP-PB	HP-UX (up to 11i), Linux

K580	1-6 PA-8200 240MHz	2/2MB	8GB	9 HSC 4 HP-PB	HP-UX (up to 11i), Linux

Notes

1. HP-UX 10.20 is the last officially supported version, certain releases of 11.00 and 11i (11.11) might also work.
2. HP-UX 11.00 is the last officially supported version, certain releases of 11i (11.11) might also work.

4.1.6 VME-Boards/Industrial

There are quite a few integrated PA-RISC systems build onto VME-boards, technically identical to some of the 715 and B-Class series workstations. They were used for data measurement and real time controlling; common uses were in the medical, industrial and military field.

Model	CPU	I/D cache per CPU	max. RAM	Expansion	OS
742i/50	PA-7100 50MHz	64/64KB	64MB		HP-UX (up to 10.20), Linux, OpenBSD
743i/64	PA-7100LC 64MHz	256KB	256MB	(2 GSC-M/4 PMC)	HP-UX (up to 11i), Linux, OpenBSD
743i/100	PA-7100LC 100MHz	256KB	256MB	(2 GSC-M/4 PMC)	HP-UX (up to 11i), Linux, OpenBSD
744/132L	PA-7300LC 132MHz	64/64KB	1GB	(2 GSC-M/4 PMC)	HP-UX (up to 11i), Linux, OpenBSD
744/165L	PA-7300LC 165MHz	64/64KB + 512KB	1GB	(2 GSC-M/4 PMC)	HP-UX (up to 11i), Linux, OpenBSD
745i/50	PA-7100 50MHz	64/64KB	128MB	4 EISA	HP-UX (up to 10.20), Linux, OpenBSD
745i/100	PA-7100 100MHz	256/256KB	256MB	4 EISA	HP-UX (up to 10.20), Linux, OpenBSD
745/132L	PA-7300LC 132MHz	64/64KB	1GB	4 EISA/4 PCI (2 GSC-M/4 PMC)	HP-UX (up to 11i), Linux, OpenBSD
745/165L	PA-7300LC 165MHz	64/64KB + 512KB	1GB	4 EISA/4 PCI (2 GSC-M/4 PMC)	HP-UX (up to 11i), Linux, OpenBSD
747i/50	PA-7100 50MHz	64/64KB	128MB	2 EISA 1 SGC 6 VME	HP-UX (up to 10.20), Linux, OpenBSD

747i/100	PA-7100 100MHz	256/256KB	256MB	2 EISA 1 SGC 6 VME	HP-UX (up to 10.20), Linux, OpenBSD
748i/64	PA-7100LC 64MHz	256KB	256MB	4 EISA(/4 PCI) (2 GSC-M/4 PMC) 6 VME	HP-UX (up to 11i), Linux, OpenBSD
748i/100	PA-7100LC 100MHz	256KB	256MB	4 EISA(/4 PCI) (2 GSC-M/4 PMC) 6 VME	HP-UX (up to 11i), Linux, OpenBSD
748i/132L	PA-7300LC 132MHz	64/64KB	1GB	4 EISA(/4 PCI) (2 GSC-M/4 PMC) 6 VME	HP-UX (up to 11i), Linux, OpenBSD
748i/165L	PA-7300LC 165MHz	64/64KB + 512KB	1GB	4 EISA(/4 PCI) (2 GSC-M/4 PMC) 6 VME	HP-UX (up to 11i), Linux, OpenBSD

4.1.7 Rack-mountable (19")

These servers were especially build for housing in 19" racks, the A-Class systems are rather flat 2U boxen while the L and R-Class are build into 7U-tall cases. They have no integrated graphics or connectors for keyboard and mouse but offer a large set of I/O-buses and slots.

Model	**height**	**CPU**	**I/D cache per CPU**	**max. RAM**	**Expansion**	**OS**
A180	2U	PA-7300LC 180MHz	64/64KB	2GB	2 GSC/PCI	HP-UX (up to 11i), Linux, NetBSD, OpenBSD
A180C	2U	PA-7300LC 180MHz	64/64KB + 1MB	2GB	2 GSC/PCI	HP-UX (up to 11i), Linux, NetBSD, OpenBSD
A400 rp2400/rp2430	2U	1 *(See Note 1)*	depends	2GB	2 PCI	HP-UX (up to 11i), Linux
A500 rp2450/rp2470	2U	1-2 *(See Note 1)*	depends	8GB	4 PCI	HP-UX (up to 11i), Linux
rp3410-2	2U	PA-8800/PA-8900 800MHz	1.5/1.5MB + 32/64MB	6GB	2 PCI-X	HP-UX (up to 11i)
rp3440-4	2U	2 PA-8800/PA-8900 800MHz/1GHz	1.5/1.5MB + 32/64MB	32GB	4 PCI-X	HP-UX (up to 11i)
rp4410-4	4U	2 PA-8800/PA-8900 800MHz/1GHz	1.5/1.5MB + 32/64MB	128B	6 PCI-X	HP-UX (up to 11i)
rp4440-8	4U	4 PA-8800/PA-8900 800MHz/1GHz	1.5/1.5MB + 32/64MB	128GB	6 PCI-X	HP-UX (up to 11i)
L1000 rp5400	7U	1-2 *(See Note 1)*	depends	8GB	5 PCI	HP-UX (up to 11i), Linux

L1500 rp5430	7U	1-2 *(See Note 1)*	depends	8GB	5 PCI	HP-UX (up to 11i)
L2000 rp5450	7U	1-4 *(See Note 1)*	depends	16GB	10 PCI	HP-UX (up to 11i), Linux
L3000 rp5470	7U	1-4 *(See Note 1)*	depends	16GB	10 PCI	HP-UX (up to 11i), Linux
N4000 rp7400	10U	1-4 *(See Note 1)*	depends	32GB	10 PCI	HP-UX (up to 11i), Linux
N4000 rp7405/rp7410	10U	2-8 *(See Note 1)*	depends	64GB	14/16 PCI	HP-UX (up to 11i)
rp7420	10U	1-8 PA-8800 900MHz/1GHz	1.5/1.5MB + 32MB	64GB	14 PCI	HP-UX (up to 11i)
rp8400/rp8410	17U	2-16 *(See Note 1)*	depends	64GB	16 PCI	HP-UX (up to 11i)
rp8420	17U	1-16 PA-8800 900MHz/1GHz	1.5/1.5MB + 32MB	128GB	16 PCI	HP-UX (up to 11i)
R380	6U	1-2 PA-8000 180MHz	1/1MB	3GB	4 EISA 1 GSC 3 EISA/GSC	HP-UX (up to 11i), Linux
R390	6U	1-2 PA-8200 240MHz	2/2MB	3GB	4 EISA 1 GSC 3 EISA/GSC	HP-UX (up to 11i), Linux

Notes

1. These systems were available in different CPU-configurations, denoted by a two-number/letter suffix as follows:

   - -36: PA-8500 360MHz with 512/1024KB on-chip I/D L1 cache each
   - -44: PA-8500 440MHz with 512/1024KB on-chip I/D L1 cache each
   - -5X: PA-8600 550MHz with 512/1024KB on-chip I/D L1 cache each
   - -6X: PA-8700 650MHz with 768/1536KB on-chip I/D L1 cache each
   - -7X: PA-8700 750MHz with 768/1536KB on-chip I/D L1 cache each
   - -8X: PA-8700 875MHz with 768/1536KB on-chip I/D L1 cache each
   - -9X: PA-8800 (dual-core) 900MHz with 1.5/1.5MB on-chip L1 and 32MB off-chip L2 cache each
   - upgrade to PA-8900 (dual-core) 800MHz-1.1GHz with 1.5/1.5MB on-chip L1 and 64MB off-chip L2 is apparently partially also possible (correct suffix and affected models unknown)

   Not all CPUs are/were available on all models.

4.1.8 Mainframe

These very large enterprise-class systems were designed for either HPC and large database processing. They offer a large range of expansion options, including a large set of CPUs and lots of RAM.

Model	CPU	I/D cache per CPU	max. RAM	Expansion	OS

T500	1-12 PA-7100 90MHz	1/1MB	3.75GB	14-112 HP-PB	HP-UX (up to 11i)
T520	1-12 PA-7150 120MHz	1/1MB	3.75GB	14-112 HP-PB	HP-UX (up to 11i)
T600	1-12 PA-8000 180MHz	1/1MB + 8MB	3.75GB	2-24 HSC 14-168 HP-PB	HP-UX (up to 11i)
V2200	4-16 PA-8200 180MHz	2/2MB	16GB	24 PCI	HP-UX (up to 11i)
V2250	4-16 PA-8200 240MHz	2/2MB	16GB	24 PCI	HP-UX (up to 11i)
V2500	2-32 PA-8500 440MHz	0.5/1MB	32GB	28 PCI	HP-UX (up to 11i)
V2600	2-32 PA-8600 552MHz	0.5/1MB	32GB	28 PCI	HP-UX (up to 11i)
SPP1000/CD *(Convex)*	2-16 PA-7100 100MHz	1/1MB	4GB	?	SPP-UX
SPP1000/XA *(Convex)*	8-128 PA-7100 100MHz	1/1MB	32GB	?	SPP-UX
SPP1200/CD *(Convex)*	2-16 PA-7200 120MHz	256/256KB	4GB	?	SPP-UX
SPP1200/XA *(Convex)*	8-128 PA-7200 120MHz	256/256KB	32GB	?	SPP-UX
SPP1600/CD *(Convex)*	2-16 PA-7200 120MHz	256/256KB	4GB	?	SPP-UX
SPP1600/XA *(Convex)*	8-128 PA-7200 120MHz	256/256KB	32GB	?	SPP-UX
Superdome	2-128 PA-8600/ PA-8700/ PA-8700+ PA-8800 PA-8900	varies	1TB	PCI-X	HP-UX (up to 11i)

4.1.9 Other Vendors

Hitachi

Hitachi had several lines of computers utilizing PA-RISC or compatible CPUs, ranging from workstations to enterprise servers. The 3050RX line of systems is comparable to HP's own 9000/700 series featuring small to medium sized workstations.

Go to the Hitachi 3050RX page

Stratus

Stratus built a line of high-availability PA-RISC based servers called *Continuum*. Different models were sold over the time, starting with PA-7100 based systems and peaking (for now) in PA-8600 models. Different operating systems were/are available, but most of these computers are able to run a normal HP-UX, besides Stratus' own FTX and VOS.

Go to the Stratus Continuum page

4.2 HP 9000/705 and 710

4.2.1 Overview

Project names:

- 705: Flounder
- 710: Bushmaster

The 705 and 710 series came out shortly after the original PA-RISC "Snakes" (720, 730 and 750). The internals of these basically were taken over, with some significant changes:

- Smaller I/D caches
- lower CPU clock rate
- different (narrower) connection to the memory subsystem
- integration of several subsystems (graphics, SCSI, Ethernet) onto a single mainboard
- reduced expansion possibilities

4.2.2 Internals

CPU

- 705: PA-7000 35MHz with 32/64KB off-chip I/D L1 cache
- 710: PA-7000 50MHz with 32/64KB off-chip I/D L1 cache

Chipset

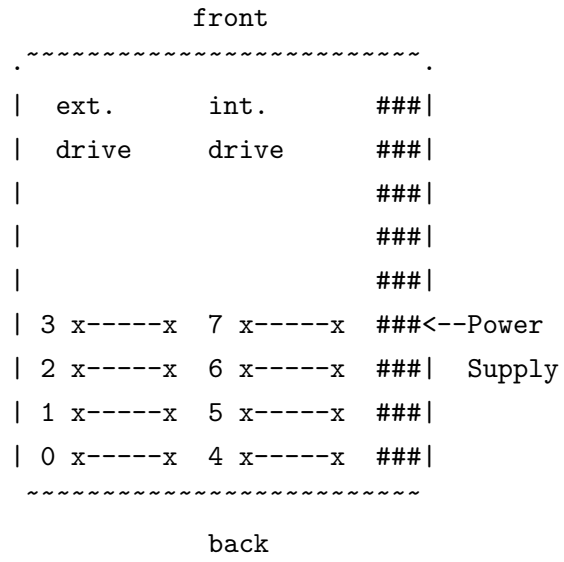
- ASP chipset, featuring:
  - NCR 53C700 8-bit single-ended SCSI-2
  - Intel 82596DX 10Mb Ethernet controller
  - WD16C552 parallel
  - NS16550A compatible serial
  - 512KB EPROM - the Boot ROM
  - 8KB EEPROM for storing system configuration status etc.
  - Intel 8042 microprocessor controlling:
    - battery backed RTC
    - system & user timers
    - HP-HIL interface
    - frontpanel system status LEDs
- Intel 82C501AD Ethernet transceiver
- PSB2160 CODEC for 8-bit mono audio

Buses

- VSC; CPU/memory bus
- GSC; system-level I/O bus
- SCSI-2 narrow single-ended bus

Memory

- HP-proprietary 72-pin SIMMs
- 8 sockets
- 16MB (4*4) (?) minimum, ?MB maximum
- Memory has to installed in *quartets*: first in the "even" slots (0,2,4,6), then in the "odd" slots (1,3,5,7):



Expansion

- No expansion slots

Drives

- One tray for a 3.5" 50-pin Narrow SE SCSI harddrive
- One tray for a half-height 5.25" 50-pin Narrow SE SCSI drive, external accessible

4.2.3 External Connectors

- 50-pin HD SCSI-2 single-ended
- two DB9 male RS232C serial
- DB25 female parallel
- 15-pin AUI 10Mbit & 10Base2 BNC Ethernet

- HD15 VGA
- HP-HIL connector for input devices
- two phone jacks (microphone, headphones)

4.2.4 Operating Systems

- HP-UX: every release from 10.01 - 10.20 works.
  - 10.20: runs ok on them, but you should get the maximum of RAM.
  - 11.00: also could work, but a) it is unsupported, b) it is very slow and c) some HP-UX patches can leave the system in an unrunnable state.
- Linux: works.

4.2.5 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
705	21.9	33.0	?	?
710	31.6	47.6	0.99	1.44

4.3 HP 9000/712

4.3.1 Overview

Project names

- 712/60: Gecko
- 712/80: King Gecko
- 712/100: King Gecko

Time of introduction

Early 1994

The design goal of the 712 was to reach performance levels of 1992-era workstations and servers at a fraction of their fabrication costs. Everything was kept simple, the case is one of the smallest Unix workstation cases, similar to the Sun SS10 and SS20 cases. Moreover, the system is very quiet, the fan of the powersupply is almost not audible, so the produced noise pretty much depends on the used SCSI harddrive. The 712 was probably the HP 9000 with the highest production count. They are readily available for a small sum of money. One big disadvantage is the limited expandability:

- maximum RAM of 128/192MB
- only one internal harddrive
- no internal CD/DAT/MO-drive
- only 8-bit graphics
- only 10Mbit Ethernet
- second Ethernet hard to find

4.3.2 Internals

CPU

- 712/60: PA-7100LC 60MHz with 1KB on-chip L1 *(See Note 1)* and 64KB off-chip L1 cache
- 712/80: PA-7100LC 80MHz with 1KB on-chip L1 *(See Note 1)* and 256KB off-chip L1 cache
- 712/100: PA-7100LC 100MHz with 1KB on-chip L1 *(See Note 1)* and 256KB off-chip L1 cache

Notes

1. The 1KB on-chip L1 cache is not really a true cache.

Chipset

- LASI ASIC, which features:
  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller

  - WD 16C522 compatible parallel
  - Harmony CD/DAT quality 16-bit stereo audio
  - NS 16550A compatible serial

- Artist graphics, 8-bit
- Intel 82503 Ethernet transceiver, media auto-selection
- CS4215 or AD1849 programmable CODECs
- WD37C65C Floppy controller
- two AM29F010 Flash EPROMs

Buses

- GSC; system level I/O bus
- SCSI-2 single-ended bus

Memory

- 72-pin ECC SIMMs
- Takes 8-32MB modules
- Either 4 (on /60 & /80 models) or 6 (on /100) sockets
- 16MB (2*8) minimum, 128MB (4*32)/ 192MB (6*32) maximum
- Memory has to be installed in pairs, starting from slot 0, which is the closest slot to the drives.

Expansion

- VRAM expansion slot for:
  - A2263-66520M - Video RAM expansion for higher resolutions/more colors
- One slot for a GIO card
- One slot for a TSIO card
- See GIO/TSIO expansion cards

Drives

- One tray for a 3.5" Fast-Narrow SE 50-pin SCSI harddrive
- One tray for a 3.5" Floppy drive with special connector

4.3.3 External Connectors

- 50-pin HD SCSI-2 Fast-Narrow single-ended
- DB9 male RS232C serial (up to 115200 baud)
- DB25 female parallel
- TP/RJ45 10Mbit Ethernet *(See Note 1)*
- 15-pin AUI 10Mbit Ethernet *(See Note 1)*
- HD15 VGA *(See Note 2)*
- two PS/2 connectors for keyboard & mouse
- three phone jacks (microphone, headphones and line-in)

Notes

1. The system automatically detects the used port.
2. You can connect almost any monitor to the VGA jack. The 712 can drive VESA compatible multisync, HP fixed-frequency and many other popular FF monitors. It also is able to produce sync on green signals.

4.3.4 ROM update

There is an firmware update available for the 712, which contains the latest version (*2.3*).

- **PF_C7120023.txt**[1] has details about the contents and installation of the patch.
- **PF_C7120023**[2] contains the patch.

4.3.5 References

- **Model 712 Technical Reference**[3] (PDF, 3.7MB)
- **Model 712 Service Handbook**[4] (PDF, 4.4MB)
- **NetBSD 712 serial console HOWTO**[5], instructions to configure your 712 to use serial console (i.e. run headless)
- **HP 9000 Model 712 Overview**[6] (PDF, HP Journal 4/95)
- **Design of the Model 712's I/O subsystem (LASI)**[7] (PDF, HP Journal 4/95)
- **Product design of the Model 712**[8] (PDF, HP Journal 4/95)
- Pinout for the AUI/RS232 Y-cable for the optional second Ethernet/serial card.

[1] http://ftp.parisc-linux.org/kernels/712/PF_C7120023.txt
[2] http://ftp.parisc-linux.org/kernels/712/PF_C7120023
[3] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37629/lpv37629.pdf
[4] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37944/lpv37944.pdf
[5] http://www.netbsd.org/Ports/hp700/serialconsole-712.html
[6] http://www.hpl.hp.com/hpjournal/95apr/apr95a1.pdf
[7] http://www.hpl.hp.com/hpjournal/95apr/apr95a4.pdf
[8] http://www.hpl.hp.com/hpjournal/95apr/apr95a9.pdf

4.3.6 Operating Systems

- HP-UX: every 32-bit release from 10.01 - 11.11 works.
  - 10.20: runs very nice on all 712s.
  - 11.00 and 11i: you'd want a 712/80 or /100 and the maximum of RAM. 712s are not the best 11.x performers though.
- NeXTSTEP: version 3.3 works fine.
- Linux: works fine.
- OpenBSD: works fine.
- NetBSD: experimental support as of 5/2005.

4.3.7 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp
712/60	67.0	85.3	2.08	2.66	18.7	23.9
712/80	97.1	123.3	3.12	3.55	28.1	32.0
712/100	117.2	144.2	3.76	4.06	33.8	36.3

4.3.8 Physical dimensions/Power

- 70*423*400 mm height*width*depth
- 8.36kg net weight
- 110W max. power input
- 1.2A max. RMS at 240V
- 2.7A max. RMS at 120V

4.4 HP 9000/715

4.4.1 Overview

Project names:

- 715/33: Scorpio Junior
- 715/50: Scorpio
- 715/64: Mirage Junior
- 715/75: Scorpio Senior
- 715/80: Mirage
- 715/100: Mirage Senior
- 715/100XC: Turnip

The HP 9000/715 range of computers can be divided into two different series:

- The 715/33, 715/50 and 715/75 were the first 715 series, they feature a PA-7100 CPU and are build around an older chipset/mainbus combo.
- The 715/64, 715/80, 715/100 and 715/100 are a bit younger and technically identical to the successful 712 series workstation.

4.4.2 Internals

CPU

- 715/33: PA-7100 33MHz with 64/64KB off-chip L1 I/D cache
- 715/50: PA-7100 50MHz with 64/64KB off-chip L1 I/D cache
- 715/64: PA-7100LC 64MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- 715/75: PA-7100 75MHz with 256/256KB off-chip L1 I/D cache
- 715/80: PA-7100LC 80MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- 715/100: PA-7100LC 100MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- 715/100XC : PA-7100LC 100MHz with 1KB on-chip I L1 and 1024KB off-chip unified I/D L1 cache

The 1KB on-chip L1 cache is not really a true cache.

Chipset

- 715/{64,80,100}:
  - LASI ASIC, which features:
    - NCR 53C710 8-bit single-ended SCSI-2
    - Intel 82596CA 10Mb Ethernet controller

        * WD 16C522 compatible parallel
        * Harmony CD/DAT quality 16-bit stereo audio
        * NS 16550A compatible serial
    - WAX ASIC, adds functionality missing in LASI, e.g. HIL, 2nd RS232 ...
    - WAX EISA bus-adaptor, connects EISA to GSC
    - Artist graphics, 8-bit
    - Intel 82503 Ethernet transceiver, media auto-selection
    - CS4215 or AD1849 programmable CODECs
    - WD37C65C Floppy controller
    - two AM29F010 Flash EPROMs

- 715/{33,50,75}:

    - ASP chipset, featuring:
        * NCR 53C700 8-bit single-ended SCSI-2
        * Intel 82596DX 10Mb Ethernet controller
        * WD 16C552 parallel
        * NS 16550A compatible serial
        * 512KB EPROM - the Boot ROM
        * 8KB EEPROM for storing system configuration status etc.
        * Intel 8042 microprocessor controlling:
            · battery backed RTC
            · system & user timers
            · audio generator
            · HP-HIL interface
            · frontpanel system status LEDs
    - Intel 82501AD Ethernet transceiver
    - Mongoose ASIC, EISA bus-adaptor
    - CRX graphics, 8-bit
    - CS4215 CODEC for 16-bit stereo audio

Buses

- GSC; system level I/O bus
- EISA; additional expansion I/O bus
- SCSI-2 single-ended narrow bus
- 715/{33,50,75}: VSC; memory/CPU bus
- 715/{33,50,75}: SGC; expansion of the mainbus to the SGC expansion card

Memory

- 72-pin ECC SIMMs
- Takes 8-32MB modules
- 8 memory sockets
- 715/33: 6 memory sockets
- 16MB (2*8) minimum, 192MB (6*32) or 256MB (8*32) maximum

Expansion

- 715/{33,50,75}: One SGC (*EISA formfactor*) expansion-slot
- 715/{64,80,100}: One GSC (*EISA formfactor*) expansion-slot
- With an adaptor-card, you also can use EISA cards in the GSC or SGC slot. Note that you only can use *one* card at a time.
- See GSC expansion-cards
- See EISA expansion-cards

Drives

- Two trays for one (1) 3.5" Fast-Narrow SE 50-pin SCSI harddrive each
- One tray for one (1) half-height 5.25" Fast-Narrow SE 50-pin SCSI drive, externally accessible

4.4.3 External Connectors

- 50-pin HD SCSI-2 single-ended Fast-Narrow
- two DB9 male RS232C serial (up to 115200 baud)
- DB25 female parallel
- 15-pin AUI 10Mbit Ethernet
- HD15 VGA
- 715/{33,50,75}: HP-HIL connector for input devices
- 715/{64,80,100}: SMD-10 connector, to connect HIL/PS2 with a special adapter [pic]
- four phone jacks (microphone, headphones and line-in and ?)

4.4.4 ROM update

There is a firmware update available for the 715/{**64,80,100**}. *This however does* **not** *work on a 715/100***XC**.

- **C7X50016.text**[9] has details about the contents and installation of the patch.
- **C7X50016.frm**[10] contains the new firmware.

[9] http://ftp.parisc-linux.org/kernels/715/C7X50016.text
[10] http://ftp.parisc-linux.org/kernels/715/C7X50016.frm

4.4.5 References

- 715/{33,50,75}: LED error codes
- 715/{64,80,100}: LED error codes
- **Model 715 Service Handbook**[11] (PDF, 5.1MB)

4.4.6 Operating Systems

- 715/{33,50,75}: HP-UX: every release from 10.01 - 10.20 works.
  - 10.20: runs nice on them.
  - 11.00: also works, but is unsupported and slow (esp. on 715/33). Some HP-UX patches can leave the system in an unrunnable state.
- 715/{64,80,100}: HP-UX: every 32-bit release from 10.01 - 11.11 works.
  - 10.20: runs very nice these 715s.
  - 11.00 and 11i: you should get the maximum of RAM. Runs OK, though 10.20 probably is faster.
- NeXTSTEP: Version 3.3 works fine.
- Linux: works.
- OpenBSD: works fine.
- NetBSD: experimental support as of 5/2005.

4.4.7 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
715/33	32.5	52.4	1.01	1.58
715/50	49.2	78.8	1.53	2.46
715/64	80.6	109.4	2.52	3.31
715/75	82.6	127.2	2.51	3.85
715/80	96.3	123.2	3.01	3.50
715/100	115.1	138.7	3.76	4.06
715/100XC	132.2	184.6	4.55	4.70

[11] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37699/lpv37699.pdf

4.5 HP 9000/725

4.5.1 Overview

Project name:

- 725/50: Spectra
- 725/75: Spectra
- 725/100: Electra

These were designated to be smaller replacements for the old 750s while still offering the same amount of I/O-Expansion options. They are technically based on their 715 counterparts.

4.5.2 Internals

CPU

- 725/50: PA-7100 50MHz with 64/64KB off-chip I/D L1 cache
- 725/75: PA-7100 75MHz with 256/256KB off-chip I/D L1 cache
- 725/100: PA-7100LC 100MHz with with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache

The 1KB on-chip L1 cache on systems with a PA-7100LC is not really a true cache.

Chipset

- 725/{50,75}: ASP chipset.
  - NCR 53C700 8-bit single-ended SCSI-2
  - Intel 82596DX 10Mb Ethernet controller
  - WD 16C552 parallel
  - NS 16550A compatible serial
  - 512KB EPROM - the Boot ROM
  - 8KB EEPROM for storing system configuration status etc.
  - Intel 8042 microprocessor
  - Intel 82501AD Ethernet transceiver
  - Mongoose ASIC, EISA bus-adaptor
  - CRX graphics, 8-bit
  - CS4215 CODEC for 16-bit stereo audio
- 725/100: LASI chipset.
  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller
  - WD 16C522 compatible parallel

  - Harmony CD/DAT quality 16-bit stereo audio
  - NS 16550A compatible serial
  - WAX ASIC, adds functionality missing in LASI, e.g. HIL, 2nd RS232 ...
  - WAX EISA bus-adaptor, connects EISA to GSC
  - Artist graphics, 8-bit
  - Intel 82503 Ethernet transceiver, media auto-selection
  - CS4215 or AD1849 programmable CODECs
  - WD37C65C Floppy controller
  - two AM29F010 Flash EPROMs

Buses

- GSC; system-level I/O bus
- EISA; additional I/O expansion bus
- 725/{50,75}: SGC; expansion of the mainbus to the "SGC" expansion card
- 725/{50,75}: VSC; memory/CPU bus
- SCSI-2 single-ended narrow bus (Fast on 725/100)

Memory

- 72-pin ECC SIMMs
- Takes 8-32MB modules
- 8 sockets
- 32MB (2*16) minimum, 256MB (8*32) maximum

Expansion

- 725/{50,75}: Three EISA expansion-slots, One slot for either a SGC (*EISA formfactor*) or EISA card.
- 725/100: One EISA expansion slot, Three slots for either GSC (*EISA formfactor*) or EISA cards.
- See EISA expansion-cards
- See GSC expansion-cards
- See SGC expansion-cards

Drives

- One tray for one 3.5" Narrow SE 50-pin SCSI harddrive
- One tray for one 3.5" Floppy drive
- Two trays for one half-height 5.25" Narrow SE 50-pin SCSI drive each, externally accessible

(725/100 supports Fast-Narrow drives)

4.5.3 External Connectors

- 50-pin HD SCSI-2 Narrow SE single-ended (Narrow-fast on 712/100)
- two DB9 male RS232C serial
- DB25 female parallel
- 15-pin AUI 10Mbit Ethernet
- HD15 VGA
- 725/{50,75}: HP-HIL connector for input devices
- 725/100: SMD-10 connector, to connect HIL/PS2 with a special adapter [pic]
- four phone jacks (microphone, headphones, line-in and ?)

4.5.4 References

- Scorpio LED error codes should also apply

4.5.5 Operating Systems

- 725/{50,75}: HP-UX: every release from 10.01 - 10.20 works.
  - 10.20: runs nice on them.
  - 11.00: also works, but a) it is unsupported, b) it is slow and c) some HP-UX patches can leave the system in an unrunnable state.
- 725/100: HP-UX: every 32-bit release from 10.01 - 11.11 works.
  - 10.20: runs very nice.
  - 11.00 and 11i: you should get the maximum of RAM. 10.20 is probably faster though.
- NeXTSTEP: Version 3.3 works fine.
- Linux: works.
- OpenBSD: works
- NetBSD: experimental support as of 5/2005.

4.5.6 Benchmarks

Model	SPEC95, int	SPEC95, fp
725/50	1.53	2.46
725/75	2.51	3.85
725/100	3.76	4.06

4.6 HP 9000/720, 730 and 750

4.6.1 Overview

Project name:

- 720: Cobra
- 730: King Cobra
- 750: Coral

These machines were the first PA-RISC workstations, called *Snakes*. Still with an "Apollo" in their model names they were introduced around June 1991, starting at $11,990 and going up to $118,190. They were build into very solid cases, consisting of interlocking exchangeable modules (*sliders*). The disk subsystem is integrated into its own "slider" while being connected to the main I/O-board via a short external cable. The 720 and 730 share the same backplane and I/O-board so you can upgrade through the exchange of the CPU-board. Upgrading to a 735 is not possible, although the case is almost identical and the CPU-board would fit mechanically. The CPU board contains three fin-cooled large-scale CMOS chips:

- the CPU
- the FPU
- the Memory and I/O Controller

4.6.2 Internals

CPU

- 720: PA-7000 50MHz with 128/256KB off-chip I/D L1 cache
- 730: PA-7000 66MHz with 128/256KB off-chip I/D L1 cache
- 750: PA-7000 66MHz with 256/256KB off-chip I/D L1 cache

Chipset

- ASP chipset, featuring:
  - NCR 53C700 8-bit single-ended SCSI-2
  - Intel 82596DX 10Mb Ethernet controller
  - WD 16C552 parallel
  - NS 16550A compatible serial
  - 512KB EPROM - the Boot ROM
  - 8KB EEPROM for storing system configuration status etc.
  - Intel 8042 microprocessor controlling:
    - battery backed RTC
    - system & user timers

    - HP-HIL interface
    - frontpanel system status LEDs

- Intel 82C501AD Ethernet transceiver
- Mongoose ASIC, EISA bus-adaptor

Buses

- VSC; CPU/memory bus
- GSC; system-level I/O bus
- EISA; additional I/O expansion bus
- SGC; expansion of the mainbus to the "SGC" expansion cards
- SCSI-2 narrow single-ended bus

Memory

- HP proprietary memory modules
- 720/730: 8 slots 750: 12 slots
- ? minimum, ? maximum

Expansion

- 720/730:
    - one SGC (*DIO-II formfactor*) expansion slot
    - one EISA slot
- 750:
    - two SGC (*DIO-II formfactor*) expansion slots
    - four EISA slots
- See SGC expansion-cards
- See EISA expansion-cards

Drives

- 720/730: one tray for two 3.5" Narrow SE 50-pin SCSI harddrives
- 750: one tray for two half-height 5.25" Narrow SE 50-pin SCSI drives and two trays for one full-height 5.25" Narrow SE 50-pin SCSI drive each

4.6.3 External Connectors

- 50-pin HD SCSI-2 single-ended
- two DB9 male RS232C serial (up to 115200 baud)
- DB25 female parallel
- 15-pin AUI 10Mbit & 10Base2 BNC Ethernet
- Graphics depend on installed SGC framebuffer
- HP-HIL connector for input devices
- Jack for beep audio

4.6.4 References:

- LED error codes
- **Model 720/730 owner's guide**[12] (PDF, 1.8MB)
- **Model 750 owner's guide**[13] (PDF, 2.1MB)

4.6.5 Operating Systems

- HP-UX: every release from 10.01 - 10.20 works.
  - 10.20: runs ok on them.
  - 11.00: also could work, but a) it is unsupported, b) it is slow and c) some HP-UX patches can leave the system in an unrunnable state.
- Linux: works.

4.6.6 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
720	36.4	58.2	1.20	2.00
730	47.8	75.4	1.50	2.30
750	48.1	75.0	1.50	2.30

[12] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37630/lpv37630.pdf
[13] http://ftp.parisc-linux.org/docs/platforms/750_owners-guide.pdf

4.7 HP 9000/735 and 755

4.7.1 Overview

Project names:

- 735/{99,125}: Hardball
- 755/{99,125}: Coral II

The 735 and 755 were designed as technical/graphical workstations or as computing servers without a framebuffer. Both 735 (desktop) and 755 (weird tower) have a very solid and massive casing which is kind of tricky to open. They also feature a large set of expansion options, buses and drives. The 735 was widely used as a FDDI node in Convex clusters.

4.7.2 Internals

CPU

- PA-7100 99MHz with 256/256KB off-chip I/D cache /
- PA-7150 125MHz with 256/256KB off-chip I/D cache

Chipset

- ASP2 chipset, featuring:
  - Cutoff ASIC, interfacing with Memory(Viper) and I/O-buses, provides address decoding, bus arbitration and interrupts
  - Shortstop ASIC, coordinates data communication between the I/O-buses and the mainbus.
  - NCR 53C700 8-bit single-ended SCSI-2
  - NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
  - Intel 82596DX 10Mb Ethernet controller
  - AMD Formac Plus Am79C830 FDDI controller
  - WD16C552 parallel, plus additional functionality provided through "Cutoff", e.g. Scanjet support.
  - NS16550A compatible serial
  - 512KB EPROM - the Boot ROM
  - 8KB EEPROM for storing system configuration status etc.
  - Intel 8042 microprocessor controlling:
    - battery backed RTC
    - system & user timers
    - audio generator
    - HP-HIL interface
    - frontpanel system status LEDs

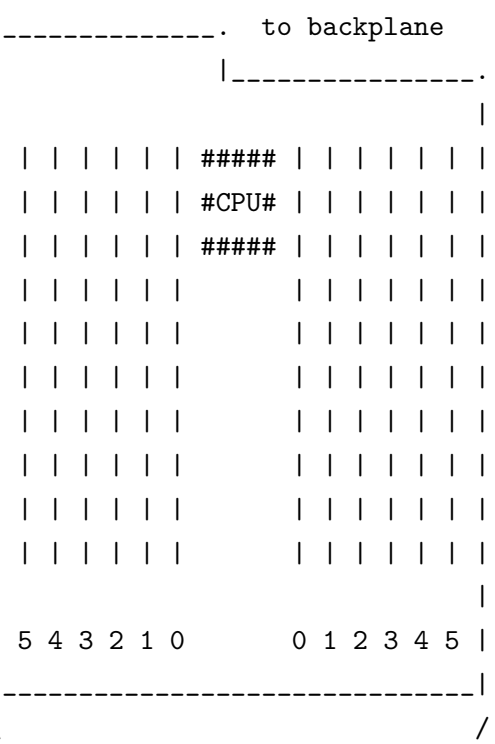
- Intel 82C501AD Ethernet transceiver
- Mongoose ASIC, EISA bus-adaptor
- CS4215 CODEC for 16-bit stereo audio

Buses

- VSC; memory/CPU bus
- GSC; system-level I/O bus
- EISA; additional I/O expansion bus
- SGC; expansion of the mainbus to the "SGC" expansion cards
- SCSI-2 narrow single-ended bus
- SCSI-2 Fast-Wide *high-voltage differential* (HVD); main storage I/O bus

Memory

- HP proprietary memory modules
- Takes 8-64MB modules
- 12 sockets
- 735: 16MB onboard, 784MB (12x64+16) maximum
- 755: 768MB (12x64) maximum
- Memory has to be installed in pairs, from bank 0 to the outside on both sides equally:



Expansion

- 735:
  - one SGC (*DIO-II formfactor*) expansion slot
  - one EISA slot
  - one daughter card slot for:
    - A2665A - FDDI SAS daughter card with MIC connector
    - A2658A - AUI Ethernet daughter card
    - A2831A - ThinLAN Ethernet daughter card
- 755:
  - two SGC (*DIO-II formfactor*) expansion slots
  - four EISA slots
- See SGC expansion-cards
- See EISA expansion-cards

Drives

- 735: one tray for either two 3.5" SCSI 68-pin Fast-Wide HVD or 50-pin narrow SE harddrives. Installed tray varies from model to model, 735/99 more often had the SE tray whereas the /125 models commonly had the F/W HVD tray.
- 755: one tray for two half-height 5.25" SCSI drives and two trays for one full-height 5.25" SCSI drive each

4.7.3 External Connectors

- 50-pin HD SCSI-2 single-ended external
- 68-pin HD SCSI-3 Fast-Wide *high-voltage differential* HVD external
- two standard RS232C serial
- DB25 parallel
- 735: 15-pin AUI or 10Base2 BNC Ethernet or FDDI SAS MIC connector
- 755: 15-pin AUI & 10Base2 BNC Ethernet connectors
- RGB BNC, depends on installed framebuffer, if at all
- HP-HIL connector for input devices
- (5) phone jacks (microphone, headphones, line-in, line-out and speaker) (*optional on 755*)

4.7.4 References

- 735/755 LED error codes
- **Model 735 Service Handbook**[14] (PDF, 7.6MB)

[14] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv38563/lpv38563.pdf

4.7.5 Operating Systems

- HP-UX: every release from 10.01 - 10.20 works.
  - 10.20: runs very nice on them.
  - 11.00: the version from March 2000 should be the last one that runs on these machines. Newer install CDs may even do not start at all. General Patch Releases from a date later than 03/2000 could make your installation unusable. 11.00 on these machines is completely unsupported from HP though.
  - 11i: 11i is officially unsupported on these systems, depending on the date of the installation CDs it might be possible to install 11i on 735/755s though. It seems the system is stable once up and running, however the patches have to be carefully reviewed as some of the SCSI patches might break the system. If booting the install CD does not work it is possible to set up an Ignite-UX install server on another HP box and netboot from that.
- NeXTSTEP: Version 3.3 works fine, but the 53C720 Fast-Wide HVD SCSI subsystem and the FDDI boards are NOT supported.
- Linux: works.
- OpenBSD: works fine, but the 53C720 Fast-Wide HVD SCSI-controller is not supported.
- NetBSD: experimental support as of 5/2005, but the 53C720 Fast-Wide HVD SCSI-controller is not supported.

4.7.6 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp
/99	3.22	4.06	29.4	35.8
/125	3.97	4.61	36.3	40.9

4.8 HP 9000/742i VME-Boards

4.8.1 Overview

Project name:

- Sidewinder

4.8.2 Internals

The *Sidewinder* is a so-called *Single Board Computer* (SBC), based on VME. It features basically the same core electronics as the 715/50 on a single board, but has fewer expansion possibilities, i.e. it takes only a small amount of RAM, has no on-board expansion slots and no graphics hardware (so a serial console has to be used). The SCSI-I/O is routed through the VME-P2 connector at the back; since the board features a VME-controller ASIC it is able to talk to other VME devices on the same bus (and control them).

CPU

- PA-7100 50MHz with 64/64KB off-chip I/D L1 cache

Chipset

- ASP chipset, featuring:
  - NCR 53C700 8-bit single-ended SCSI-2
  - Intel 82596DX 10Mb Ethernet controller
  - WD 16C552 parallel
  - NS 16550A compatible serial
  - 512KB EPROM - the Boot ROM
  - 8KB EEPROM for storing system configuration status etc.
  - Intel 8042 microprocessor controlling:
    - battery backed RTC
    - system & user timers
    - audio generator
    - HP-HIL interface
    - frontpanel system status LEDs
- Intel 82501AD Ethernet transceiver
- Mongoose ASIC, EISA bus-adaptor
- CRX graphics, 8-bit
- CS4215 CODEC for 16-bit stereo audio
- VME bus-adaptor

Buses

- VSC; memory/CPU bus
- GSC; system-level I/O bus
- VME bus
- SCSI-2 narrow single-ended bus.

Memory

- 72-pin ECC SIMMs
- Takes 8-32MB modules
- 2 slots
- 16MB (2*8) minimum, 64MB (2*32) maximum

Expansion

- no

4.8.3 External Connectors

- 50-pin HD SCSI-2 Fast-Narrow single-ended
- two DB9 male RS232C serial
- DB25 female parallel
- DB15 15-pin AUI 10Mbit Ethernet

4.8.4 References

- **742i Owner's Guide**[15] (PDF, 1.5MB)

4.8.5 Operating Systems

- HP-UX: every 32-bit release from 9.01 to 10.20 works.
- Linux: should run.

4.8.6 Benchmarks

Model	SPEC95, int	SPEC95, fp
742i/50	1.53	2.46

4.8.7 Physical dimensions/Power

- 40*233*160mm height*width*depth

[15] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00299/lpv00299.pdf

- height of 2 VMEbus slots
- 0.91kg weight
- 35W @ +5V DC
- 0.12W @ +12V DC
- 0.12W @ -12V DC

4.9 HP 9000/743i and 744 VME Boards

4.9.1 Overview

Project names - uname(1):

- 743i/64 - Anole-64
- 743i/100 - Anole-100
- 744/132L - Anole-132L
- 744/165L - Anole-165L

These *Anole* named computers are so called VME *Single Board Computers* (SBCs). The whole system processing unit alongside with the memory and several other I/O-controllers sit on a single-height 2U VME-board, which needs a fitting VME-cage to function properly. The board would plug into one of the VME-slots of the latter, which in turn would provide power and route some parts of the I/O, in this case SCSI, through the so-called P2-connector.

The SBCs also feature a small set of expansion cards, which plug into any of the available expansion boards and include GSC-mezzanine (GSC-M) and PCI-mezzanine (PMC) cards. It is also possible to use an EISA or PCI-cage on several of HP's own systems based on the 743i and 744. Since the board also features an VME-controller it can talk to and control other VME-cards plugged into the same VME-bus/cage. Of note is that some of the pins on the P2-VME connector on the back are used to route GSC-bus traffic trough to several of the expansion options. VME-cages have to be properly jumpered to support this, i.e. to don't interfere with this. Also, it is dangerous to use these boards in a VXI-cage since some of the VXI-pins carry voltage which would result in burned ASICs on the GSC-bus.

The 743i is technically closely based on the corresponding 715 models, the 744 partially on the B132L/B160L workstations.

The 743i boards are used in the 748i industrial workstations, the 744 boards in the 745 and 748 industrial workstations.

4.9.2 Internals

CPU

- 743i/64: PA-7100LC 64MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- 743i/100: PA-7100LC 64MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- 744/132L: PA-7300LC 132MHz with 64/64KB on-chip I/D L1 cache
- 744/165L: PA-7300LC 165MHz with 64/64KB on-chip I/D L1 and 512KB off-chip unified I/D L2 cache

The 1KB on-chip L1 cache on systems with a PA-7100LC is not really a true cache.

Chipset

- LASI ASIC, which features:

  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller
  - WD 16C522 compatible parallel
  - Harmony CD/DAT quality 16-bit stereo audio
  - NS 16550A compatible serial

- WAX ASIC, adds functionality missing in LASI, e.g. HIL, 2nd RS232 ...
- WAX EISA bus-adaptor, connects EISA to GSC
- Dino GSC-to-PCI bridge
- 744: Phantom PseudoBC GSC+ port
- 744: Visualize-EG ("Graffiti") graphics
- Intel 82503 Ethernet transceiver, media auto-selection
- CS4215 or AD1849 programmable CODECs
- VME-controller
- PCMCIA-controller

Buses

- GSC bus,
- optional EISA bus,
- optional PCI-32/33 bus,
- VME bus
- SCSI-2 Fast-Narrow single-ended bus.

Memory

- Use special ECC mezzanine cards
- 743i and 744 use different cards
- 743i: Takes 8-64MB special ECC mezzanine cards
- 744: Takes 16-256MB special ECC mezzanine cards
- Up to four cards are supported
- 743i: 8MB minimum, 256MB maximum amount of RAM
- 744: 16MB minimum, 1GB maximum amount of RAM

Expansion

- Two sites for GSC-mezzanine (GSC-M) cards, requires the A4219A GSC Expansion kit, **or**

- two sites for PCI-mezzanine (PMC) cards, requires the A4504A PMC bridge board. (Two additional PMC-sites can be obtained through the addition of the A4509A PMC Expander board to the above).
- See GSC/GSC-M expansion cards

4.9.3 External Connectors

- 50-pin HD SCSI-2 Fast-Narrow single-ended
- two micro-DB9 male RS232C serial *(See Note 1)*
- micro-DB25 female parallel *(See Note 1)*
- micro-DB15 15-pin AUI 10Mbit Ethernet *(See Note 1)*
- micro-DB15 VGA graphics *(See Note 1)*
- two PS/2 connectors for keyboard & mouse
- micro-DB9 for audio breakout *(See Note 1)*

Notes

1. These micro-connectors need original HP-conversion cables to provide the normal-sized version of their respective connector.

4.9.4 ROM update

There is an firmware update available for the 744, which contains the latest version (*4.4*).

- **PF_C7440044.txt**[16] has details about the contents and installation of the patch.
- **PF_C7440044**[17] contains the patch.

4.9.5 References

- **743 Owner's Guide**[18] (PDF, 1.8MB)
- **743, 744 and 748 Technical Reference Manual**[19] (PDF, 2.2MB)
- **744 Owner's Guide**[20] (PDF, 1.4MB)
- **Installing the A4505A PCI Module Upgrade**[21] (PDF, 0.3MB)
- **Installing the A4504A PMC Bridge Adapter and A4509A Expansion Adapter**[22] (PDF, 0.6MB)
- **Installing Model 743 RAM Boards**[23] (PDF, 0.2MB)

[16] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_C7440044.txt
[17] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_C7440044
[18] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv38556/lpv38556.pdf
[19] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00265/lpv00265.pdf
[20] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00271/lpv00271.pdf
[21] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00284/lpv00284.pdf
[22] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00276/lpv00276.pdf
[23] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00298/lpv00298.pdf

- **Installing Model 744 RAM Cards**[24] (PDF, 0.3MB)
- **VME Services for HP-UX 10 and 11**[25] (PDF, 1.3MB)

4.9.6 Operating Systems

- HP-UX: every 32-bit release from 10.20 - 11.11 works.
  - 10.20: runs nicely.
  - 11.00 and 11i: runs nicely.
- Linux: should run.
- OpenBSD: should run.

4.9.7 Benchmarks

Model	SPEC95, int	SPEC95, fp
743i/64	2.52	3.31
743i/100	3.76	4.03
744/123L	6.45	6.70
744/165L	7.90	7.64

[24] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00274/lpv00274.pdf
[25] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00267/lpv00267.pdf

4.10 HP 9000/745i and 747i

4.10.1 Overview

Project names:

- 745i/50: Pace
- 747i/50: Pace
- 745i/100: Fast Pace
- 747i/100: Fast Pace

These *Pace* named models were one of the first HPPA workstations for industrial/medical use. They are technically very similar to the older 715s and 725s while being build in ruggedized, rack-mountable cases. The CPU and I/O-controllers sit on a VME-SBC (single-board-computer) which is identical on both 745i and 747i. The latter systems are build in an even bigger case and feature VME-slots, which the 745i do not have. Both have a HP-IB interface, which was used mainly for controlling and/or instrumental use. Most interestingly these machines have two pairs of LED-banks, one at the front and the other directly on the CPU-board on the back.

4.10.2 Internals

CPU

- 745i/50: PA-7100 50MHz with 64/64KB off-chip I/D L1 cache
- 747i/50: PA-7100 50MHz with 64/64KB off-chip I/D L1 cache
- 745i/100: PA-7100 100MHz with 256/256KB off-chip I/D L1 cache
- 747i/100: PA-7100 100MHz with 256/256KB off-chip I/D L1 cache

Chipset

- ASP chipset, featuring:
  - NCR 53C700 8-bit single-ended SCSI-2
  - Intel 82596DX 10Mb Ethernet controller
  - WD 16C552 parallel
  - NS 16550A compatible serial
  - 512KB EPROM - the Boot ROM
  - 8KB EEPROM for storing system configuration status etc.
  - Intel 8042 microprocessor controlling:
    - battery backed RTC
    - system & user timers
    - audio generator
    - HP-HIL interface

    - frontpanel system status LEDs

- Intel 82501AD Ethernet transceiver
- Mongoose ASIC, EISA bus-adaptor
- CRX graphics, 8-bit
- HP-IB controller
- 747i: VME controller
- PSB2160 CODEC for 8-bit mono audio

Buses

- VSC; memory/CPU bus
- GSC; system-level I/O bus
- EISA; I/O expansion bus
- HP-IB bus (IEEE-488); peripheral bus
- SCSI-2 narrow single-ended bus
- 747i: SGC; expansion of the mainbus to the "SGC" expansion slot
- 747i: VME bus

Memory

- 72-pin ECC SIMMs
- Takes 8-32MB modules (/100 models take 64MB modules)
- 4 sockets
- /50 models: 16MB (2*8) minimum, 128MB (4*32) maximum
- /100 models: 16MB (2*8) minimum, 256MB (4*64) maximum

Expansion

- 745i: Four EISA expansion-slots.
- 747i: Two EISA expansion-slots, One SGC (*DIO-II formfactor*) expansion slot, 6 VME slots.
- See EISA expansion-cards
- See SGC expansion-cards

Drives

- one bay for an external-accessible 5.25" half-height SCSI drive
- one bay for an external-accessible 3.5" SCSI drive or floppy
- one bay for a 3.5" SCSI drive

4.10.3 External Connectors

- 50-pin HD SCSI-2 single-ended
- two DB9 male RS232C serial
- DB25 female parallel
- 15-pin AUI 10Mbit Ethernet
- HD 15 VGA
- HP-HIL connector for input devices
- HP-IB for peripherals
- three phone jacks (microphone-in, headphone-out and speaker-out)

4.10.4 References

- LED error codes from older 715s should apply
- **700i Industrial Workstations Owner's Guide**[26] (PDF, 1,6MB)

4.10.5 Operating Systems

- HP-UX: every release from 10.01 - 10.20 works.
  - 10.20: runs nice on them.
  - 11.00: also works, but a) it is unsupported, b) it is slow and c) some HP-UX patches can leave the system in an unrunnable state.
- NeXTSTEP: Version 3.3 could work.
- Linux: works.
- OpenBSD: works.

4.10.6 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
/50	36	72	1.53	2.46
/100	81	138	3.22	4.06

4.10.7 Physical dimensions/Power

745i:

- 175*425*412mm height*width*depth
- 18.6kg net weight
- 350W max. power input

[26] http://www.hp.com/products1/vmesystems/support/doc_vme/A2628-90014.pdf

747i:

- 310*425*412mm heigth*width*depth
- 29kg net weight
- 700W max. power input

4.11 HP 9000/748i and 748 Workstations

4.11.1 Overview

Project names - uname(1):

- 748i/64 - Anole-64
- 748i/100 - Anole-100
- 748/132L - Anole-132L
- 748/165L - Anole-165L

The 748i and 748 *ruggedized workstations* are in fact 743i and 744 VME-Boards in a heavy, large VME-case, which provides the neccessary I/O-facilities:

- six 6U-VME-slots for additional I/O-boards
- room for up to four SCSI-devices, all of which can be accessed from the outside
- a four-slot EISA or PCI cage

4.11.2 Internals

CPU

- 748i/64: PA-7100LC 64MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- 748i/100: PA-7100LC 64MHz with 1KB on-chip I L1 and 256KB off-chip unified I/D L1 cache
- 748/132L: PA-7300LC 132MHz with 64/64KB on-chip I/D L1 cache
- 748/165L: PA-7300LC 165MHz with 64/64KB on-chip I/D L1 and 512KB off-chip unified I/D L2 cache

The 1KB on-chip L1 cache on systems with a PA-7100LC is not really a true cache.

Chipset

- LASI ASIC, which features:
  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller
  - WD 16C522 compatible parallel
  - Harmony CD/DAT quality 16-bit stereo audio
  - NS 16550A compatible serial
- WAX ASIC, adds functionality missing in LASI, e.g. HIL, 2nd RS232 ...
- WAX EISA bus-adaptor, connects EISA to GSC
- Dino GSC-to-PCI bridge
- 748: Phantom PseudoBC GSC+ port

- 748: Visualize-EG ("Graffiti") graphics
- Intel 82503 Ethernet transceiver, media auto-selection
- CS4215 or AD1849 programmable CODECs
- VME-controller
- PCMCIA-controller

Buses

- GSC bus,
- optional EISA bus,
- optional PCI-32/33 bus,
- VME bus
- SCSI-2 Fast-Narrow single-ended bus.

Memory

- Use special ECC mezzanine cards
- 748i and 748 use different cards
- 748i: Takes 8-64MB special ECC mezzanine cards
- 748: Takes 16-256MB special ECC mezzanine cards
- Up to four cards are supported
- 748i: 8MB minimum, 256MB maximum amount of RAM
- 748: 16MB minimum, 1GB maximum amount of RAM

Expansion

- Two sites for GSC-mezzanine (GSC-M) cards, requires the A4219A GSC Expansion kit, **or**
- two sites for PCI-mezzanine (PMC) cards, requires the A4504A PMC bridge board. (Two additional PMC-sites can be obtained through the addition of the A4509A PMC Expander board to the above).
- See GSC/GSC-M expansion cards
- Six 6U-VME slots
- Either four EISA or four PCI slots in a separate I/O-cage

4.11.3 External Connectors

- 50-pin HD SCSI-2 Fast-Narrow single-ended
- two micro-DB9 male RS232C serial *(See Note 1)*
- micro-DB25 female parallel *(See Note 1)*

- micro-DB15 15-pin AUI 10Mbit Ethernet *(See Note 1)*
- micro-DB15 VGA graphics *(See Note 1)*
- two PS/2 connectors for keyboard & mouse
- micro-DB9 for audio breakout *(See Note 1)*
- on configurations with an EISA-cage: HIL-connector

Notes

1. These micro-connectors need original HP-conversion cables to provide the normal-sized version of their respective connector.

4.11.4 ROM update

There is an firmware update available for the 744-board (used in 748), which contains the latest version (*4.4*).

- **PF_C7440044.txt**[27] has details about the contents and installation of the patch.
- **PF_C7440044**[28] contains the patch.

4.11.5 References

- **Model 748 Workstation Owner's Guide**[29] (PDF, 3.2MB)
- **Service Handbook Model 748**[30] (PDF, 3.6MB)
- Refer also to the 743i and 744 page

4.11.6 Operating Systems

- HP-UX: every 32-bit release from 10.20 - 11.11 works.
  - 10.20: runs very nice. *For a B180L+ you need at least ACE 9707*
  - 11.00 and 11i: runs nice, you'd want at least 256MB RAM.
- Linux: should run.
- OpenBSD: should run.

4.11.7 Benchmarks

Model	SPEC95, int	SPEC95, fp
748i/64	2.52	3.31
748i/100	3.76	4.03
748/123L	6.45	6.70
748/165L	7.90	7.64

[27] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_C7440044.txt
[28] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_C7440044
[29] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00281/lpv00281.pdf
[30] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00282/lpv00282.pdf

4.11.8 Physical dimensions/Power

- 324*425*419mm height*width*depth
- 29.0kg weight
- Two redundant 350W power supplies

4.12 HP 9000/A-Class

4.12.1 Overview

Project names:

- A180: Staccato
- A180C: Staccato

Introduction:

- September 1998

The PA-7300LC based A180 and A180C were one of the latest PA1.1-powered HP 9000 servers. They are quite small and also rackmountable. Designated as *Enterprise Internet Servers* they do not offer any video output, only serial console or a *Secure Web Console*.

4.12.2 Internals

CPU

- A180: PA-7300LC 180MHz with 64/64KB on-chip I/D L1 cache
- A180C: PA-7300LC 180MHz with 64/64KB on-chip I/D L1 and 1MB off-chip unified L2 cache

The additional 1MB L2 cache is the only difference between both systems. This cache is upgradeable through two DIMM slots near the CPU.

Chipset

- LASI ASIC, which features:
  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller
  - NS 16550A compatible serial
- Dino GSC-to-PCI bridge
- Phantom PseudoBC GSC+ port
- DEC 21142/43 10/100BaseT PCI Ethernet

Buses

- GSC+; general system-level I/O bus
- PCI; high performance device I/O bus
- SCSI-2 Fast-Narrow single-ended; main storage I/O bus

Memory

- 72-pin ECC EDO SIMMs, 60ns or faster.
- Takes 64-256MB modules
- 8 slots
- 128MB (2*64) minimum, 2048MB (8*256) maximum

Expansion

- Two slots for either GSC (*EISA formfactor*) or PCI cards
- See GSC expansion-cards

Drives

- One tray for two 3.5" Fast-Narrow 50-pin SCSI harddrives

4.12.3 External Connectors

- 50-pin HD SCSI-2 single-ended
- DB9 male RS232C serial
- TP/RJ45 10/100Mbit Ethernet
- TP/RJ45 10Mbit Ethernet "Web Console"

4.12.4 References:

- **A180 User's Manual**[31] (PDF, 0.9MB)

4.12.5 ROM update

There is a firmware update available for the A180[C], which contains the latest version (*39.32*).

- **PF_CSTD3932.txt**[32] has details about the contents and installation of the patch.
- **PF_CSTD3932**[33] contains the patch.

4.12.6 Operating Systems

- HP-UX: every 32-bit release from 10.20 - 11.11 works.
  - 10.20: runs very nice.
  - 11.00 and 11i: run nice, you'd want at least 256MB RAM, more is better.
- Linux: works fine.

[31] http://docs.hp.com/hpux/pdf/Aclassdoc00.pdf
[32] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CSTD3932.txt
[33] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CSTD3932

- OpenBSD: works fine.
- NetBSD: experimental support as of 5/2005.

4.12.7 Benchmarks

Model	SPEC95, int	SPEC95, fp
A180	?	?
A180C	9.22	8.60

4.13 HP A400 and A500 (rp24xx) Servers

4.13.1 Overview

Project names

- A400-36 (rp2400): Crescendo DC-360
- A400-44 (rp2400): Crescendo DC-440
- A400-5X (rp2400): Crescendo DC-550
- A400-6X (rp2430): Crescendo DC-650 W2
- A400-7X (rp2430): Crescendo DC-750 W2
- A400-8X (rp2430): ?
- A400-9X (rp2430): ?
- A500-36 (rp2450): Crescendo 360
- A500-44 (rp2450): Crescendo 440
- A500-5X (rp2450): Crescendo 550
- A500-6X (rp2470): Crescendo 650 W2
- A500-7X (rp2470): Crescendo 750 W2
- A500-8X (rp2470): ?
- A500-9X (rp2470): ?

Introduction

- Mai 2000

These systems were the 64-bit successors to the popular A180 rack-servers. The chassis remained superficially the same – it is still a 2U rack-mountable case, but the interior changed significantly. The various models are sported by 64-bit PA-RISC CPUs in different variations, but are all using large on-chip L1 caches. The I/O-subsystem was redesigned around the Astro memory/CPU-controller and several Elroy PCI bridges, which control the various PCI-slots and integrated I/O-devices. The difference between the A400 and A500 is that the latter are SMP-capable and can use more memory-modules and PCI-cards.

They also feature an advanced version of the *Secure Web Console* found in the earlier A180 systems. It is called *Guardian Service Processor* (GSP) and can be reached with pressing `Ctrl-b`. It can be used for a wide range of administrative tasks; in the **References** section further below is a link to a detailed command summary.

Original prices of the entry version were $4,600 for the A400-44 and $9,200 for a single-CPU A500-5X.

4.13.2 Internals

CPU

The A400 systems are uniprocessor systems while the A500 support up to 2-way SMP. The following table lists the various suffixes denoting the different theoretically possible CPU-configurations. Upgrading from one configuration to another could require the replacement of other parts besides the processor, e.g. the mainboard or power supply.

- A400: one CPU
- A500: up to two CPUs

- -36: PA-8500 360MHz with 512/1024KB on-chip I/D L1 cache each
- -44: PA-8500 440MHz with 512/1024KB on-chip I/D L1 cache each
- -5X: PA-8600 550MHz with 512/1024KB on-chip I/D L1 cache each
- -6X: PA-8700 650MHz with 768/1536KB on-chip I/D L1 cache each
- -7X: PA-8700 750MHz with 768/1536KB on-chip I/D L1 cache each
- -8X: PA-8700 875MHz with 768/1536KB on-chip I/D L1 cache each
- -9X: PA-8800 (dual-core) 900MHz/1GHz with 1.5/1.5MB on-chip L1 and 32MB off-chip L2 cache each

Chipset

- Astro memory/Runway controller
- 4 Elroy PCI bridges
- 2 HP Diva Serial [GSP] Multiport UARTs
- DEC 21142/43 Fast Ethernet controller *(Tulip)*
- Symbios Logic 53C876 SCSI controller, (includes 2 Symbios Logic 53C875 cores with each one Ultra-Wide SCSI-2 bus)
- Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

- Runway; CPU/memory bus
- PCI-64/33; high-performance I/O bus
- 3 PCI-64/66; high-performance I/O buses
- SCSI-2 Ultra-Narrow single-ended bus
- 2 SCSI-3 Ultra2-Wide LVD buses

Memory

- ECC SDRAM DIMMs
- Take 256MB/512MB/1GB modules
- 8 slots, A400 can only use first 4 of those
- 256MB (1*256) minimum, A400: 2GB (4*512MB) maximum; A500: 8GB (8*1GB) maximum.

Expansion

- Four PCI 64-bit/66MHz, 5V slots (two slots on A400)
- Two of those slots are "*Twin-turbo*" slots, which means that each slots sits on its own dedicated about 500MB/s bandwith "rope".
- The other two slots are "*shared*" slots, which means that they share a single 250MB/s "rope" (XXX?). (these slots are only available on A500s)

Drives

- Two trays for each one 3.5" Ultra2-Wide LVD SCSI harddrives with 80-pin SCA connector which require a special spud to be plugged into the system.

4.13.3 External Connectors

- 50-pin HD SCSI-2 Ultra-Narrow single-ended
- 68-pin HD SCSI-3 Ultra2-Wide LVD(xxx)
- DB25 male RS232C serial for console/UPS (a break-out cable which converts to three DB9 plugs)
- TP/RJ45 10/100Mbit Ethernet
- TP/RJ45 10Mbit Ethernet for Secure Web Console/GSP

4.13.4 ROM update

There is an firmware update available which contains the latest version (*43.50*).

- **PF_CHAW4350.txt**[34] has details about the contents and installation of the patch.
- **PF_CHAW4350.tar.gz**[35] contains the patch.

There is also an firmware update available for the GSP (service processor) on rp2430 and rp2470 systems which contains the latest version (*C.02.14*).

- **PF_CHARGSPC0214.txt**[36] has details about the contents and installation of the patch.
- **PF_CHARGSPC0214.tar.gz**[37] contains the patch.

[34] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CHAW4350.txt
[35] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CHAW4350.tar.gz
[36] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CHARGSPC0214.txt
[37] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CHARGSPC0214.tar.gz

4.13.5 References

- **Hardware manual**[38] (PDF)
- **Doug's HP 9000 - GSP Notes Page**[39] with a detailed description of the available GSP commands.

4.13.6 Operating Systems

- HP-UX: Only 64-bit 11.00 and 11i releases run.
- Linux: works, but the SMP-support on some models supposedly is a bit flaky and not all CPU-configurations are supported.

4.13.7 Physical dimensions/Power

- 95*482*635mm height*width*depth
- rack-mounted: 2U height, 482*774mm width*depth
- 22.68kg net weight

[38] http://www.docs.hp.com/hpux/onlinedocs/2411/rp24xx_customer.pdf
[39] http://web.tampabay.rr.com/batcave/GSPinfo.htm

4.14 HP 9000/B-Class

4.14.1 Overview

Project names - uname(1):

- B132L[+]: Merlin L2 - 9000/778
- B160L: Merlin L2 - 9000/778
- B180L+: Merlin L2 - 9000/778

These are very nice, small entry-level workstations. Still based on a 32-bit PA-RISC CPU they were designed as successors to the successful 715 workstations with better performance and I/O-expandability. They were developed alongside the C-Class workstations, sharing a similar casing concept but integrating more functionality onto on single mainboard to save manufacturing costs. The +-models (B132L+, B180L+) differ from the others in having Ultra-Wide SE SCSI and 10/100Mb Ethernet rather than Fast-Wide HVD SCSI and only 10Mb Ethernet.

4.14.2 Internals

CPU

- B132L: PA-7300LC 132MHz with 64/64KB int. L1 (+ 1MB ext. L2)
- B132L+: PA-7300LC 132MHz with 64/64KB int. L1 (+ 1MB ext. L2)
- B160L: PA-7300LC 160MHz with 64/64KB int. L1 (+ 1MB ext. L2)
- B180L+: PA-7300LC 180MHz with 64/64KB int. L1 (+ 1MB ext. L2)

The external L2 cache SRAM is optional and is installed in two DIMM slots below the CPU socket. The modules must be of equal size. Usually, these systems come with 2 512KB modules, totalling in 1MB L2.

Chipset

- LASI ASIC, which features:
  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller
  - WD 16C522 compatible parallel
  - Harmony CD/DAT quality 16-bit stereo audio
  - NS 16550A compatible serial
- WAX ASIC, adds functionality missing in LASI, e.g. HIL, 2nd RS232 ...
- WAX EISA bus-adaptor, connects EISA to GSC
- Dino GSC-to-PCI bridge
- Phantom PseudoBC GSC+ port

- Visualize-EG ("Graffiti") graphics
- Intel 82503 Ethernet transceiver, media auto-selection
- CS4215 or AD1849 programmable CODECs
- WD37C65C Floppy controller
- B132L, B160L: NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
- B132L+, B180L+: Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controller
- B132L+, B180L+: DEC 21142/43 (*Tulip*) Fast-Ethernet controller

Buses

- GSC; general system-level I/O bus
  - B132L (both): 33MHz
  - B160L: 40MHz
  - B180L+: 36MHz
- EISA; additional expansion I/O bus
- PCI-32/33; high-performance device I/O bus
- SCSI-2 Fast-Narrow single-ended bus
- B132L, B160L: SCSI-2 Fast-Wide *high-voltage differential* main storage I/O bus
- B132L+, B180L+: SCSI-2 Ultra-Wide single-ended; main storage I/O bus

Memory

- 72-pin ECC SIMMs, 60ns or faster
- Takes 16-256MB modules (latest firmware-rev needed)
- 6 slots
- 32MB (2*16) minimum, 1.5GB (6*256) maximum

Expansion

- B132L, B160L:
  - One slot for either a GSC (*EISA formfactor*) or PCI 32-bit/33MHz, 3.3V card
  - One slot for either a GSC (*EISA formfactor*), PCI 32-bit/33MHz, 3.3V or EISA card
- B132L+, B180L+:
  - One slot for either a GSC (*EISA formfactor*) or PCI 32-bit/33MHz, 5V card
  - One slot for either a GSC (*EISA formfactor*), PCI 32-bit/33MHz, 5V or EISA card
- See GSC expansion-cards

- See EISA expansion-cards
- I/O-slots:

```
TOP
1     [#####]          [#####] PCI-32/33 or GSC
2     [#####]                  PCI-32/33 or
   [##########]        [#####] EISA or GSC
BOTTOM
```

Drives

- One tray for a 68-pin half-height 3.5" SCSI harddrive, either Fast-Wide *high-voltage differential* (B132L, B160L) or Ultra-Wide SE (+-models)
- One tray for a 3.5" Floppy drive
- One tray for a 50-pin half-heigth 5.25" Fast-Narrow 50-pin SE SCSI drive, external accessible, can also accomodate a harddrive.

4.14.3 External Connectors

- 50-pin HD SCSI-2 Fast-Narrow single-ended
- B132L, B160L: 68-pin HD SCSI-2 Fast-Wide *high-voltage differential*
- B132L+, B180L+: 68-pin HD SCSI-3 Ultra-Wide single-ended
- two DB9 male RS232C serial
- DB25 female parallel
- B132L, B160L: TP/RJ45 10Mbit Ethernet
- B132L+, B180L+: TP/RJ45 10/100Mbit Ethernet
- 15-pin AUI 10Mbit Ethernet
- EVC graphics port *(See Note 1)*
- two PS/2 connectors for keyboard & mouse
- four phone jacks (microphone, headphones, line-in and line-out)

Notes

1. You need a special HP adapter-cable to convert this EVC-port to either BNC or HD15 VGA

4.14.4 ROM update

There is an firmware update available for the B-Class, which contains the latest version (*6.1*).

- **PF_CB1X0061.txt**[40] has details about the contents and installation of the patch.
- **CB1X0061.frm**[41] contains the patch.

[40] http://ftp.parisc-linux.org/kernels/b180/PF_CB1X0061.txt
[41] http://ftp.parisc-linux.org/kernels/b180/CB1X0061.frm

4.14.5 References

- LED error codes
- **B-Class Owner's Guide**[42] (PDF, 1.5MB)
- **B-Class Service Handbook**[43] (PDF, 0.9MB)
- **B-Class Low-Cost Workstation description**[44] (PDF, HP Journal 7/97)

4.14.6 Operating Systems

- HP-UX: every 32-bit release from 10.20 - 11.11 works.
  - 10.20: runs very nicely. *For a B180L+ you need at least ACE 9707*
  - 11.00 and 11i: run nicely.
- Linux: works fine.
- OpenBSD: works fine, but the 53C720 Fast-Wide HVD SCSI-controller found on the B132L and B160L is not supported.
- NetBSD: experimental support as of 5/2005, but the 53C720 Fast-Wide HVD SCSI-controller found on the B132L and B160L is not supported.

4.14.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp
B132	6.45	6.70	58.1	60.3
B132+	6.84	7.17	61.5	64.6
B160L	7.75	7.56	69.7	68.1
B180L+	9.22	9.43	83.0	84.8

4.14.8 Physical dimensions/Power

- 116*445*452mm height*width*depth
- 16kg net weight, 18kg fully loaded
- 300W max. power input
- 3A max. RMS at 240V
- 5A max. RMS at 120V

[42] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37741/lpv37741.pdf
[43] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37927/lpv37927.pdf
[44] http://www.hpl.hp.com/hpjournal/97jun/jun97a11.pdf

4.15 HP Visualize B2000 and B2600

4.15.1 Overview

Project names - uname(1):

- B2000: Kazoo - 9000/785
- B2600: Piccolo W+ - 9000/785

These workstations were aimed at the graphics workstations market, equipped with the 64-bit PA-8500 or PA-8600 featuring large on-chip L1 caches. The B2000 features normally the former CPU and is shipped in a small tower enclosure whereas the B2600 is shipped in a desktop casing, featuring the PA-8600 CPU. The architecture was a major change from those of its predecessors, e.g. the C200 et al. New I/O devices were integrated, the LASI I/O chip was dumped, together with the GSC bus. All device I/O now sits on various PCI buses, human I/O devices are connected to USB ports.

4.15.2 Internals

CPU

- B2000: PA-8500 400MHz with 512/1024KB on-chip I/D L1 cache
- B2600: PA-8600 500MHz with 512/1024KB on-chip I/D L1 cache

(there are some B2000s shipped with/upgraded to PA-8600 (PCXW+) processors)

Chipset

- Astro memory/Runway controller
- 2 Elroy PCI bridges
- National 87560 (SuperI/O), handling USB, RS232, parallel, floppy and IDE
- National 87415 IDE controller
- National USB controller
- Analog Devices AD1889 sound chip (on B2600 the audio card is optional)
- DEC 21142/43 Fast Ethernet controller *(Tulip)*
- Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller
- B2000: Visualize FXe graphics

Buses

- Runway; CPU/memory bus
- PCI-32/33; device I/O bus
- PCI-64/33; high-performance I/O bus
- SCSI-3 Ultra2-Wide LVD bus; main storage I/O
- IDE bus; removable device-I/O (can partially boot from CD-ROM, e.g. HP-UX)

Memory

- 278-pin 120MHz ECC SD-RAM DIMMs
- Takes 128MB-1GB modules
- 4 slots
- 128MB (1*128) minimum, 4GB (4*1GB) maximum

Expansion

- Two PCI 64-bit/33MHz, 5V slots (clocked at 66MHz on B2600)
- Two PCI 32-bit/33MHz, 5V slots
- B2000: I/O-slots

```
TOP
1  [##################]       PCI-64/33, 5V
2  [##################]       PCI-64/33, 5V
3  [#########]               PCI-32/33, 5V
4  [#########]               PCI-32/33, 5V
BOTTOM
```

- B2600: I/O-slots

```
TOP
1  [#########]               PCI-32/33, 5V, short PCI cards
2  [#########]               PCI-32/33, 5V, short PCI cards
3  [##################]       PCI-64/33, 5V, short and full-length cards
4  [##################]       PCI-64/33, 5V, short and full-length cards
BOTTOM
```

Drives

- One tray for two 3.5" Ultra2-Wide LVD SCSI harddrives with 80-pin SCA connector
- One tray for a 3.5" Floppy drive
- One tray for a half-heigth 5.25" IDE drive, external accessible

4.15.3 External Connectors

- B2000: HD15 VGA
- 2 DB9 male RS232C serial
- DB25 female parallel
- TP/RJ45 10/100Mbit Ethernet
- 2 USB ports for keyboard & mouse

- 4 audio jacks (microphone, headphones, line-in and line-out) (on B2600 the audio card is optional)

4.15.4 ROM update

There is an firmware update available for the B2000, which contains the latest version (*5.0*).

- **PF_CBCJ0050.txt**[45] has details about the contents and installation of the patch.
- **PF_CBCJ0050**[46] contains the patch.

4.15.5 References

- **B2000 Service Handbook**[47] (PDF, 8.8MB)
- **B2000 Owner's Guide**[48] (PDF, 2.6MB)
- **VISUALIZE Workstation Memory Subsystem**[49] (PDF, 120KB)

4.15.6 Operating Systems

- HP-UX: every release from 10.20 *ACE 9907* - 11.11 works.
  - 10.20: very fast You need at least *ACE 9907*.
  - 11.00 and 11i: run nicely.
- Linux: works.

4.15.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp	SPEC2000, int	SPEC2000, fp
B2000	31.80	52.40	286	472	313	321
B2600					380	397

4.15.8 Physical dimensions/Power

B2000:

- 445*229*495mm height*width*depth
- rack-mounted: 6U height, 451*665mm width*depth
- 18.6kg net weight, 21.4kg fully loaded
- 620W max. power input
- 3.5A max. RMS at 240V

[45] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050.txt
[46] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050
[47] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37671/lpv37671.pdf
[48] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37670/lpv37670.pdf
[49] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37826/lpv37826.pdf

- 8.0A max. RMS at 120V

B2600:

- 127*425*457mm height*width*depth
- rack-mounted: 127*483*495mm width*depth
- 18.2kg net weight, 20.2kg fully loaded
- 1.8A max. RMS at 240V
- 3.6A max. RMS at 120V

4.16 HP 9000/C100 and C110

4.16.1 Overview

Project names:

- C100: Raven T - 9000/777
- C110: Raven T - 9000/777

These were meant to be graphics workstations equipped with the new PA-7200 CPU. They have a similar case to that of the 735, it is build of interlocking modules, so you easily could take out the I/O board, the MPU board etc.. These machines were aimed at CAD/CAM/3D-modelling so their architecture was chosen in this light.

4.16.2 Internals

CPU

- C100: PA-7200 100MHz with 256/256KB off-chip I/D L1 cache and 2KB on-chip "assist" L1 cache
- C110: PA-7200 120MHz with 256/256KB off-chip I/D L1 cache and 2KB on-chip "assist" L1 cache

The "assist" cache is not really a true cache.

Chipset

- LASI ASIC, which features:
  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller
  - WD 16C522 compatible parallel
  - Harmony CD/DAT quality 16-bit stereo audio
  - NS 16550A compatible serial
- 2 U2/Uturn-IOA BC Runway ports
- WAX ASIC, adds functionality missing in LASI, e.g. HIL, 2nd RS232 ...
- WAX EISA bus-adaptor, connects EISA to GSC
- GSC Graphics
- Intel 82C503 Ethernet transceiver, media auto-selection
- CS4215 or AD1849 programmable CODECs
- WD37C65C Floppy controller
- NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2

Buses

- Runway; CPU/memory bus
- GSC; general system-level I/O bus
- EISA; additional expansion I/O bus
- SCSI-2 single-ended bus
- SCSI-2 Fast-Wide *high-voltage differential*; main storage I/O bus

Memory

- 72-pin ECC SIMMs, 60ns or faster
- Bus width: 128 data bits with 16 check bits
- Up to 8-way interleaving
- 400MB/s (C100), 480MB/s (C110) peak bandwidth
- Takes 16-128MB modules
- 8 slots
- 32MB (2*16) minimum, 1GB (8*128) maximum

Expansion

- One slot for a GSC (*EISA formfactor*) card
- Three slots for either GSC (*EISA formfactor*) or EISA cards
- See GSC expansion-cards
- See EISA expansion-cards
- I/O-slots:

```
TOP
1  [###########]       [#####] EISA or GSC
2  [###########]       [#####] EISA or GSC
3  [###########]       [#####] EISA or GSC (for secondary graphics)
4                      [#####] GSC      (for primary graphics)
BOTTOM
```

Drives

The disk-slider can accomodate up to three SCSI-drives and one floppy-drive simultaneously, the internal cabling (usually) includes one Wide-SCSI cable with three 68-pin connectors and a HVD-terminator at the end, one Narrow-SCSI with one 50-pin connector and one cable for the floppy.

The *Narrow-SCSI* cable is normally used for the external-accessible half-height 5.25" CD/DAT-drive, although it is of course also possible to connect a 50-pin SE harddrive. The cable can also be

easily replaced with a variant with more connectors to use up to three 50-pin SE harddrives. The PDC can boot off these SE-drives.

The *Wide-SCSI* cable is normally used for the internal 3.5" 68-pin Fast-Wide *high-voltage differential* system drives. Up to three harddrives can be installed in the cage, which leaves no room for an external-accessible CD/DAT-drive though. The Fast-Wide drives are also bootable by the PDC.

A standard configuration could look like this:

- Two 3.5" 68-pin Fast-Wide differential (HVD) SCSI harddrives,
- one 3.5" Floppy-drive and
- one external-accessible half-height 5.25" SCSI-drive (CD/DAT).

4.16.3 External Connectors

- 50-pin HD SCSI-2 single-ended
- 68-pin HD SCSI-3 Fast-Wide *differential* (HVD)
- 2 DB9 male RS232C serial (up 460.8Kb/s)
- DB25 female parallel
- TP/RJ45 10Mbit Ethernet
- 15-pin AUI 10Mbit Ethernet
- Graphics port depend on installed video adapter
- 2 PS/2 connectors for keyboard and mouse
- HP-HIL for input device loop
- 4 phone jacks (microphone, headphones, line-in and ?)

4.16.4 ROM update

There is a firmware update available for the C110, which contains the latest version (*1.3*).

- **PF_CC110013.txt**[50] has details about the contents and installation of the patch.
- **PF_CC110013**[51] contains the patch.

There is also a firmware update available for the C100 and C110, which contains the latest version (*1.2*).

- **PF_CC1X0012.txt**[52] has details about the contents and installation of the patch.
- **PF_CC1X0012**[53] contains the patch.

[50] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC110013.txt
[51] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC110013
[52] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu//PF_CC1X0012.txt
[53] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu//PF_CC1X0012

4.16.5 Operating Systems

- HP-UX: every 32-bit release from 10.20 - 11.11 works.
  - 10.20: runs very nicely.
  - 11.00 and 11i: runs nicely
- Linux: works fine.
- OpenBSD works fine, but the 53C720 Fast-Wide HVD SCSI-controller is not supported, so you need to use Fast-Narrow SE SCSI drives.

4.16.6 References

- LED error codes
- **C100/110 Owners Guide**[54] (PDF, 1.6MB)
- **C100/110 Service Handbook**[55] (PDF, 1.5MB)
- **C100 to C110 CPU upgrade**[56] (PDF, 0.2MB)
- **C100, C110 to C160L CPU upgrade**[57] (PDF, 0.5MB)
- **C100, C110 to C160, C180 CPU upgrade**[58] (PDF, 0.5MB)
- **C100, C110, C160, C180 to C200 CPU upgrade**[59] (PDF, 0.5MB)

4.16.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPECrate95, int	SPECrate95, fp
C100	4.98	6.59	44.8	59.4
C110	6.00	8.14	54.0	73.3

4.16.8 Physical dimensions/Power

- 138*539*447 mm height*width*depth
- 16.7kg net weight, 21.1kg fully loaded
- 555W max. power input
- 5.0A max. RMS at 240V
- 9.5A max. RMS at 120V

[54] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37672/lpv37672.pdf
[55] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37947/lpv37947.pdf
[56] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37945/lpv37945.pdf
[57] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37952/lpv37952.pdf
[58] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37949/lpv37949.pdf
[59] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37951/lpv37951.pdf

4.17 HP 9000/C132L and C160L

4.17.1 Overview

Project names - uname(1):

- C132L: Raven L2 - 9000/779
- C160L: Raven L2 - 9000/779

These were meant to be entry-level workstations equipped with the new PA-7300LC CPU. They have a similar case to that of the 735, it is build of interlocking modules, so you easily could take out the I/O board, the MPU board etc.. These machines were aimed at CAD/CAM/3D-modelling so their architecture was chosen in this light.

4.17.2 Internals

CPU

- C132L: PA-7300LC 132MHz with 64/64KB on-chip I/D L1 (and 1MB off-chip unified L2) cache
- C160L: PA-7300LC 160MHz with 64/64KB on-chip I/D L1 (and 1MB off-chip unified L2) cache

The off-chip L2 cache SRAM is optional and is installed in two DIMM slots below the CPU socket. The modules must be of equal size. Usually, these systems come with 2 512KB modules, totalling in 1MB L2 cache.

Chipset

- LASI ASIC, which features:
  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller
  - WD 16C522 compatible parallel
  - Harmony CD/DAT quality 16-bit stereo audio
  - NS 16550A compatible serial
- WAX ASIC, adds functionality missing in LASI, e.g. HIL, 2nd RS232 ...
- WAX EISA bus-adaptor, connects EISA to GSC
- Dino GSC-to-PCI bridge
- Phantom PseudoBC GSC+ port
- Visualize-EG graphics
- Intel 82C503 Ethernet transceiver, media auto-selection
- CS4215 or AD1849 programmable CODECs
- WD37C65C Floppy controller
- NCR 53C720 16-bit Fast-Wide *differential* (HVD) SCSI-2

Buses

- Runway; CPU/memory bus
- GSC-2; general system-level I/O bus
- EISA; additional expansion I/O bus
- PCI-32/33; high-performance device I/O bus
- SCSI-2 single-ended bus
- SCSI-2 Fast-Wide *differential*; main storage I/O bus

Memory

- 72-pin ECC SIMMs, 60ns or faster
- Bus width: 128 data bits with 16 check bits
- Up to 8-way interleaving
- Takes 16-256MB modules
- 12 slots
- 32MB (2*16) minimum, 2GB maximum

Expansion

- Two slots for either GSC (*EISA formfactor*) or EISA cards
- One slot for either a PCI 32-bit/33MHz, 3V or EISA card
- One slot for a PCI 32-bit/33MHz, 3V card
- Slot layout:

```
TOP
1:  [##########]       [#####]  - EISA or GSC
2:  [##########]       [#####]  - EISA or GSC
3:      [#####]                 - PCI-32/33 3V or
    [##########]                  EISA
4:      [#####]                 - PCI-32/33
BOTTOM
```

- See GSC expansion-cards
- See EISA expansion-cards

Drives

The disk-slider can accomodate up to three SCSI-drives and one floppy-drive simultaneously, the internal cabling (usually) includes one Wide-SCSI cable with three 68-pin connectors and a HVD-terminator at the end, one Narrow-SCSI with one 50-pin connector and one cable for the floppy.

The *Narrow-SCSI* cable is normally used for the external-accessible half-height 5.25" CD/DAT-drive, although it is of course also possible to connect a 50-pin SE harddrive. The cable can also be easily replaced with a variant with more connectors to use up to three 50-pin SE harddrives. The PDC can boot off these SE-drives.

The *Wide-SCSI* cable is normally used for the internal 3.5" 68-pin Fast-Wide *high-voltage differential* system drives. Up to three harddrives can be installed in the cage, which leaves no room for an external-accessible CD/DAT-drive though. The Fast-Wide drives are also bootable by the PDC.

A standard configuration could look like this:

- Two 3.5" 68-pin Fast-Wide differential (HVD) SCSI harddrives,
- one 3.5" Floppy-drive and
- one external-accessible half-height 5.25" SCSI-drive (CD/DAT).

4.17.3 External Connectors

- 50-pin HD SCSI-2 single-ended
- 68-pin HD SCSI-3 Fast-Wide *differential* (HVD)
- two DB9 male RS232C serial (up 460.8Kb/s)
- DB25 female parallel
- TP/RJ45 10Mbit Ethernet
- 15-pin AUI 10Mbit Ethernet
- EVC graphics port *(See Note 1)*
- two PS/2 connectors for keyboard and mouse
- HP-HIL for input device loop
- four phone jacks (microphone, headphones, line-in and ?)

Notes

1. You need a special HP adapter-cable to convert this EVC-port to either BNC or HD15 VGA

4.17.4 ROM update

There is a firmware update available for the C160L, which contains the latest version (*5.8*).

- **PF_CB1X0058.txt**[60] has details about the contents and installation of the patch.
- **PF_CB1X0058**[61] contains the patch.

[60] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CB1X0058.txt
[61] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CB1X0058

4.17.5 References

- LED error codes
- **C160L Owners Guide**[62] (PDF, 1.6MB)
- **C-Class Service handbook**[63] (PDF, 1.6MB)
- **C100, C110 to C160L CPU upgrade**[64] (PDF, 0.5MB)

4.17.6 Operating Systems

- HP-UX: every 32-bit release from 10.20 - 11.11 works.
  - 10.20: runs very nice.
  - 11.00 and 11i: runs nicely.
- Linux: works fine.
- OpenBSD: works fine, but the 53C720 Fast-Wide HVD SCSI-controller is not supported.
- NetBSD: experimental support as of 5/2005, but the 53C720 Fast-Wide HVD SCSI-controller is not supported.

4.17.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp
C132L	6.45	6.70	58.1	60.3
C160L	7.75	7.56	7.75/7.56	69.7/68.1

4.17.8 Physical dimensions/Power

- 138*539*447 mm height*width*depth
- 16.7kg net weight, 21.1kg fully loaded
- 525W max. power input
- 5.0A max. RMS at 240V
- 9.5A max. RMS at 120V

[62] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37959/lpv37959.pdf
[63] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37954/lpv37954.pdf
[64] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37952/lpv37952.pdf

4.18 HP 9000/C160 and C180

4.18.1 Overview

Project names - uname(1):

- C160: Raven U - 9000/780
- C180: Raven U - 9000/780

The C180 is also sometimes referred to as **C180XP**.

These were meant to be graphics workstations equipped with the new PA-8000 CPU. They have a similar case to that of the 735, it is build of interlocking modules, so you easily could take out the I/O board, the MPU board etc.. These machines were aimed at CAD/CAM/3D-modelling so their architecture was chosen in this light.

4.18.2 Internals

CPU

- C160: PA-8000 160MHz with 512/512KB off-chip I/D L1 cache
  - 128-bit wide bus to cache
  - 2.56GB/s I-fetch
  - 2.56GB/s D-load (16-Byte), 1.26GB/s D-store (8-Byte)
- C180: PA-8000 180MHz with 1024/1024KB off-chip I/D L1 cache
  - 128-bit wide bus to cache
  - 2.88GB/s I-fetch
  - 2.88GB/s D-load (16-Byte), 1.44GB/s D-store (8-Byte)

Chipset

- LASI ASIC, which features:
  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller
  - WD 16C522 compatible parallel
  - Harmony CD/DAT quality 16-bit stereo audio
  - NS 16550A compatible serial
- 2 U2/Uturn-IOA BC Runway ports
- WAX ASIC, adds functionality missing in LASI, e.g. HIL, 2nd RS232 ...
- WAX EISA bus-adaptor, connects EISA to GSC
- Dino GSC-to-PCI bridge

- Visualize-EG graphics
- Intel 82C503 Ethernet transceiver, media auto-selection
- CS4215 or AD1849 programmable CODECs
- WD37C65C Floppy controller
- NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2

Buses

- Runway; CPU/memory bus
- GSC-2; general system-level I/O bus
- EISA; additional expansion I/O bus
- PCI-32/33; high-performance device I/O bus
- SCSI-2 single-ended bus
- SCSI-2 Fast-Wide *high-voltage differential*; main storage I/O bus

Memory

- 72-pin ECC SIMMs, 60ns or faster
- Bus width: 128 data bits with 16 check bits
- Up to 8-way interleaving
- 960MB/s peak bandwidth
- Takes 16-256MB modules (needs latest firmware-revision for large modules)
- 12 slots
- 32MB (2*16) minimum, 3GB (12*256) maximum

Expansion

- One slot for either a GSC (*EISA formfactor*) or PCI 32-bit/33MHz, 3.3V card
- One slot for either a GSC (*EISA formfactor*), EISA or PCI 32-bit/33MHz, 3.3V card
- Two slots for either GSC (*EISA formfactor*) or EISA cards
- See GSC expansion-cards
- See EISA expansion-cards
- I/O-slots:

```
TOP
1  [##########]       [#####] EISA or GSC
2  [##########]       [#####] EISA or GSC
3     [#####]                 PCI-32/33, 3.3V or
```

```
   [##########]       [#####] EISA or GSC
4     [#####]         [#####] PCI-32/33, 3.3V or GSC
BOTTOM
```

Drives

The disk-slider can accomodate up to three SCSI-drives and one floppy-drive simultaneously, the internal cabling (usually) includes one Wide-SCSI cable with three 68-pin connectors and a HVD-terminator at the end, one Narrow-SCSI with one 50-pin connector and one cable for the floppy.

The *Narrow-SCSI* cable is normally used for the external-accessible half-height 5.25" CD/DAT-drive, although it is of course also possible to connect a 50-pin SE harddrive. The cable can also be easily replaced with a variant with more connectors to use up to three 50-pin SE harddrives. The PDC can boot off these SE-drives.

The *Wide-SCSI* cable is normally used for the internal 3.5" 68-pin Fast-Wide *high-voltage differential* system drives. Up to three harddrives can be installed in the cage, which leaves no room for an external-accessible CD/DAT-drive though. The Fast-Wide drives are also bootable by the PDC.

A standard configuration could look like this:

- Two 3.5" 68-pin Fast-Wide differential (HVD) SCSI harddrives,
- one 3.5" Floppy-drive and
- one external-accessible half-height 5.25" SCSI-drive (CD/DAT).

4.18.3 External Connectors

- 50-pin HD SCSI-2 single-ended
- 68-pin HD SCSI-3 Fast-Wide *differential* (HVD)
- 2 DB9 male RS232C serial (up 460.8Kb/s)
- DB25 female parallel
- TP/RJ45 10Mbit Ethernet
- 15-pin AUI 10Mbit Ethernet
- EVC graphics port *(See Note 1)*
- 2 PS/2 connectors for keyboard and mouse
- HP-HIL for input device loop
- 4 phone jacks (microphone, headphones, line-in and ?)

Notes

1. You need a special HP adapter-cable to convert this EVC-port to either BNC or HD15 VGA

4.18.4 ROM update

There is a firmware update available for the C160 and C180, which contains the latest version (*6.2*).

- **PF_CC2X0062.text**[65] has details about the contents and installation of the patch.
- **PF_CC2X0062.frm**[66] contains the patch.

4.18.5 Operating Systems

- HP-UX: every release from 10.20 - 11.11 works.
  - 10.20: runs very nice.
  - 11.00 and 11i: run also very nicely in either 32 or 64-bit mode. You need *EP9808* to run a 64-bit 11.0 environment on a machine with a 64-bit PA-8000.
- Linux: works fine.
- OpenBSD: runs fine (in 32-bit mode).

4.18.6 References

- LED error codes
- **C-Class Owners Guide**[67] (PDF, 1.5MB)
- **C100, C110 to C160, C180 CPU upgrade**[68] (PDF, 0.5MB)
- **C160 to C180 CPU upgrade**[69] (PDF, 0.2MB)
- **C100, C110, C160, C180 to C200 CPU upgrade**[70] (PDF, 0.5MB)

4.18.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp
C160	10.40	16.30	93.6	147
C180	11.80	18.70	107	169

4.18.8 Physical dimensions/Power

- 138*539*447 mm height*width*depth
- 16.7kg net weight, 21.1kg fully loaded
- 525W max. power input
- 5.0A max. RMS at 240V
- 9.5A max. RMS at 120V

[65] ftp://ftp.parisc-linux.org/kernels/c200/CC2X0062.text
[66] ftp://ftp.parisc-linux.org/kernels/c200/CC2X0062.frm
[67] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37673/lpv37673.pdf
[68] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37949/lpv37949.pdf
[69] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37957/lpv37957.pdf
[70] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37951/lpv37951.pdf

4.19 HP 9000/C200, C240 and C360

4.19.1 Overview

Project names - uname(1):

- C200: Raven U+ - 9000/782
- C240: Raven U+ - 9000/782
- C360: Raven W - 9000/785

These are also sometimes referred to as C200+ and C240+.

These were aimed at the graphics workstations market, equipped with the 64-bit PA-8200 and PA-8500 CPUs. They have a similar case to that of the old 735 - build of interlocking modules so the I/O board, the MPU board etc. can be easily taken out. These machines were aimed at CAD/CAM/3D-modelling so their architecture was chosen in this light. They are really fast machines with impressive FP power. They are nicely expendable and built like a tank so could have really long uptimes. Interesting is the CPU building block, which really looks impressive.

These machines tend to have problems with the power supply (PSU). Some just refuse to start up any longer. Michael Kukat researched the problem and summarized his solution in an posting to the USENET: **HP C200/C240/C360 Power Supply problems - solved**[71].

4.19.2 Internals

CPU

- C200: PA-8200 200MHz with 512/1024KB off-chip I/D L1 cache
- C240: PA-8200 236MHz with 2048/2048KB off-chip I/D L1 cache
- C360: PA-8500 367MHz with 512/1024KB on-chip I/D L1 cache

Chipset

- LASI ASIC, which features:
  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller
  - WD 16C522 compatible parallel
  - Harmony CD/DAT quality 16-bit stereo audio
  - NS 16550A compatible serial
- 2 U2/Uturn-IOA BC Runway ports
- WAX ASIC, adds functionality missing in LASI, e.g. HIL, 2nd RS232 ...
- WAX EISA bus-adaptor, connects EISA to GSC
- Dino GSC-to-PCI bridge

[71] http://groups.google.de/groups?selm=20041127170355.H89099@calchas.unixiron.org

- Cujo GSC-to-PCI bridge
- Intel 82C503 Ethernet transceiver, media auto-selection
- CS4215 or AD1849 programmable CODECs
- WD37C65C Floppy controller
- Symbios Logic 53C875 16-bit Ultra-Wide SCSI-2 controller
- DEC 21142/43 *(Tulip)* Fast-Ethernet controller

Buses

- Runway; CPU/memory bus
- GSC-2; general system-level I/O bus
- EISA (*only when specially ordered*); additional expansion I/O
- PCI-32/33; device I/O bus
- PCI-64/66; high-performance device I/O bus
- SCSI-2 Fast-Narrow single-ended bus
- SCSI-2 Ultra-Wide single-ended bus; main storage I/O

Memory

- 72-pin ECC EDO SIMMs, 50ns or faster (should run with 60ns modules too)
- Takes 16-256MB modules (needs latest firmware-rev)
- 12 slots
- 32MB (2*16) minimum, 3GB (12*256) maximum

Expansion

- Three slots for either GSC (*EISA formfactor*) or PCI cards
- One slot for either a GSC (*EISA formfactor*), PCI or EISA card
- Two of the PCI slots are PCI 32-bit/33MHz, 5V; the other two PCI 64-bit/66MHz, 3.3V. Some system don't have the optional EISA slot
- See GSC expansion-cards
- See EISA expansion-cards
- I/O-slots:

```
TOP
1     [#####]                 PCI-32/33, 5V or
   [##########]       [#####] EISA or GSC
2     [#########]     [#####] PCI-64/66, 3.3V or GSC
3     [#####]         [#####] PCI-32/33, 5V or GSC
```

```
4     [##########]     [#####] PCI-64/66, 3.3V or GSC
BOTTOM
```

Drives

The disk-slider can accomodate up to three SCSI-drives and one floppy-drive simultaneously, the internal cabling (usually) includes one Wide-SCSI cable with three 68-pin connectors and a SE-terminator at the end, one Narrow-SCSI with one 50-pin connector and one cable for the floppy.

The *Narrow-SCSI* cable is normally used for the external-accessible half-height 5.25" CD/DAT-drive, although it is of course also possible to connect a 50-pin SE harddrive. The cable can also be easily replaced with a variant with more connectors to use up to three 50-pin SE harddrives. The PDC can boot off these SE-drives.

The *Wide-SCSI* cable is normally used for the internal 3.5" 68-pin Ultra-Wide SE system drives. Up to three harddrives can be installed in the cage, which leaves no room for an external-accessible CD/DAT-drive though. The Ultra-Wide drives are also bootable by the PDC.

A standard configuration could look like this:

- Two 3.5" 68-pin Ultra-Wide single-ended (SE) SCSI harddrives,
- one 3.5" Floppy-drive and
- one external-accessible half-height 5.25" SCSI-drive (CD/DAT).

4.19.3 External Connectors

- 50-pin HD SCSI-2 Fast-Narrow single-ended
- 68-pin HD SCSI-3 Ultra-Wide single-ended
- 2 DB9 male RS232C serial
- DB25 female parallel
- TP/RJ45 10/100Mbit Ethernet
- 15-pin AUI 10Mbit Ethernet
- 2 PS/2 connectors for keyboard & mouse
- 4 phone jacks (microphone, headphones, line-in and ?)

4.19.4 ROM update

There is an firmware update available for the C200 & C240, which contains the latest version (*6.3*).

- **PF_CC2X0063.txt**[72] has details about the contents and installation of the patch.
- **PF_CC2X0063**[73] contains the patch.

There is also an firmware update available for the C360, which contains the latest version (*1.5*).

[72] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC2X0063.txt
[73] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC2X0063

- **PF_CC360015.txt**[74] has details about the contents and installation of the patch.
- **PF_CC360015**[75] contains the patch.

4.19.5 References

- LED error codes
- **C-Class Owners Guide**[76] (PDF, 1.5MB)
- **C-Class Service handbook**[77] (PDF, 1.6MB)
- **C100, C110, C160, C180 to C200 CPU upgrade**[78] (PDF, 0.5MB)
- **C200 to C240 CPU upgrade**[79] (PDF, 0.2MB)
- **C200, C240 to C360 CPU upgrade**[80] (PDF, 0.2MB)
- **HP C200/C240/C360 Power Supply problems - solved**[81].

4.19.6 Operating Systems

- HP-UX: every release from 10.20 *ACE 9707* - 11.11 works.
  - 10.20: very fast You need at least *ACE 9707*.
  - 11.00 and 11i: run nicely. You need *EP9808* to run a 64-bit 11.0 environment
- Linux: works fine.
- OpenBSD: runs fine (in 32-bit mode).

4.19.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPECrate95, int	SPECrate95, fp
C200	14.20	21.40	129	193
C240	17.10	25.40	156	229
C360	26.00	28.10	234	252

4.19.8 Physical dimensions/Power

- 138*539*447mm height*width*depth
- 17.7kg net weight, 22.7kg fully loaded
- 880W max. power input
- 5A max. RMS at 240V

[74] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC360015.txt
[75] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CC360015
[76] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37673/lpv37673.pdf
[77] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37954/lpv37954.pdf
[78] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37951/lpv37951.pdf
[79] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37960/lpv37960.pdf
[80] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37961/lpv37961.pdf
[81] http://groups.google.de/groups?selm=20041127170355.H89099@calchas.unixiron.org

- 10A max. RMS at 120V

4.20 HP Visualize B1000, C3000 and C3600

4.20.1 Overview

Project names - uname(1):

- B1000: AllegroLow - 9000/785
- C3000: AllegroHigh - 9000/785
- C3600: Allegro W+ - 9000/785
- C3650: Allegro W2 - 9000/785
- C3700: Allegro W2 - 9000/785
- C3750: Allegro W2 - 9000/785

These workstations were aimed at the graphics workstations market, equipped with the 64-bit PA-8500 featuring large on-chip L1 caches. The C3600 is essentially a C3000 upgraded to a PA-8600 CPU, the C3700 is the same, but upgraded to a PA-8700 CPU. There were additionally various more upgraded models, e.g. the C3650 and the C3750, the former with a faster PA-8700 CPU, the latter with an even faster PA-8700+ CPU. The architecture was a major change from those of its predecessors, e.g. the C200 et al. New I/O devices were integrated, the LASI I/O chip was dumped, together with the GSC bus. All device I/O now sits on various PCI buses, human I/O devices are connected to USB ports. The case also was a major redesign.

4.20.2 Internals

CPU

- B1000: PA-8500 300MHz with 512/1024KB on-chip I/D L1 cache
- C3000: PA-8500 400MHz with 512/1024KB on-chip I/D L1 cache
- C3600: PA-8600 552MHz with 512/1024KB on-chip I/D L1 cache
- C3650: PA-8700 625MHz with 768/1536KB on-chip I/D L1 cache
- C3700: PA-8700 750MHz with 768/1536KB on-chip I/D L1 cache
- C3750: PA-8700+ 875MHz with 768/1536KB on-chip I/D L1 cache

Chipset

- Astro memory/Runway controller
- 4 Elroy PCI bridges
- National 87560 *(SuperI/O)*, handling USB, RS232, parallel, floppy and IDE
- National 87415 IDE controller
- National USB controller
- Analog Devices AD1889 sound chip

- DEC 21142/43 Fast Ethernet controller *(Tulip)*
- Symbios Logic 53C896 SCSI-3 controller

Buses

- Runway; CPU/memory bus
- PCI-32/33; device I/O bus
- PCI-64/33; high-performance device I/O bus
- PCI-64/66; high-performance graphics I/O bus
- C37x0: PCI-64/100; high-performance graphics I/O bus
- SCSI-2 Ultra-Narrow single-ended bus; external I/O
- SCSI-3 Ultra2-Wide LVD bus; storage-I/O
- IDE bus; removable device-I/O (can partially boot from CD-ROM, e.g. HP-UX)

Memory

- 278-pin 120MHz ECC SDRAM DIMMs
- Takes 128/256/512/1024MB modules (needs latest firmware revision)
- 8 slots
- 128MB (1*128) minimum, 8GB (8*1GB) maximum

Expansion

- One PCI 64-bit/66MHz, 3.3V slot (clocked at 100MHz on C37x0 systems)
- Three PCI 64-bit/33MHz, 5V slots
- Two PCI 32-bit/33MHz, 5V slots
- I/O-slots:

```
TOP
1  [##################]       PCI-64/33, pci0, 5V
2  [##################]       PCI-64/66, pci1, 3.3V (for primary graphics) 1
3  [##################]       PCI-64/33, pci0, 5V
4  [##################]       PCI-64/33, pci2, 5V (for secondary graphics)
5  [#########]               PCI-32/33, pci3, 5V
6  [#########]               PCI-32/33, pci3, 5V
BOTTOM
```

Notes

1. On C37x0 systems this is a PCI-64/100 slot.

Drives

- One tray for two 3.5" Ultra2-Wide LVD SCSI harddrives with 80-pin SCA connector
- One tray for a 3.5" Floppy drive
- One tray for a half-heigth 5.25" IDE drive, external accessible

4.20.3 External Connectors

- 50-pin HD SCSI-2 Ultra-Narrow single-ended
- 68-pin HD SCSI-3 Ultra2-Wide LVD
- two DB9 male RS232C serial
- DB25 female parallel
- TP/RJ45 10/100Mbit Ethernet
- two USB ports for keyboard & mouse
- four phone jacks (microphone, headphones, line-in and line-out)

4.20.4 ROM update

There is a firmware update available for the **PA-8500 and PA-8600**-based B1000, C3000 and C3600 which contains the latest version (*5.0*).

- **PF_CBCJ0050.txt**[82] has details about the contents and installation of the patch.
- **PF_CBCJ0050**[83] contains the patch.

A different firmware update is provided for the **PA-8700**-based C37x0 systems (version 2.0):

- **PF_CCJ70020.txt**[84] has details about the contents and installation of the patch.
- **PF_CCJ70020**[85] contains the patch.

4.20.5 References

- **B1000/C3x00 Owner's Guide**[86] (PDF, 4.9MB)
- **B1000/C3x00 Service Handbook**[87] (PDF, 3.2MB)
- **VISUALIZE Workstation Memory Subsystem**[88] (PDF, 120KB)

[82] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050.txt
[83] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050
[84] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CCJ70020.txt
[85] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CCJ70020
[86] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37930/lpv37930.pdf
[87] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37739/lpv37739.pdf
[88] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37826/lpv37826.pdf

4.20.6 Operating Systems

- HP-UX: every release from 10.20 *ACE 9907* - 11.11 works.
  - 10.20: very fast You need at least *ACE 9907*.
  - 11.00 and 11i: run nicely. You need at least *ACE 9911*.
- Linux: works.

4.20.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp	SPEC2000, int	SPEC2000, fp
B1000	23.90	39.30	217	378		
C3000	31.80	52.40	287	471	313	321
C3600	42.00	64.00	379	576	432	433
C3650	?	?			508	542
C3700	?	?			604	576
C3750	?	?			678	674

4.20.8 Physical dimensions/Power

- 445*229*495 mm height*width*depth
- rack-mounted: 6U height, 451*665mm width*depth
- 20.9kg net weight, 25.4kg fully loaded
- 805W max power input
- 3.8A max RMS at 240V
- 7.4A max RMS at 120V

4.21 HP C8000

4.21.1 Overview

The c8000 is the latest (and probably last too) PA-RISC powered workstation HP offers, it is driven by one or two of dual-core PA-8800 *Mako* processors and features an impressive array of system and I/O-options. The heart of the system is the HP *zx1* chipset, which also supports Itanium processors. It is supposedly possible to exchange the PA-CPUs for IA64 (Itanium) CPUs. The system is build in a very sleek, silent tower casing and is also available as a rack-mount option.

4.21.2 Internals

CPU

- 1-2 (two-core) PA-8800 900MHz-1GHz with 1.5MB/1.5MB on-chip I/D L1 cache and 32MB off-chip L2 cache each **or**
- 1-2 (two-core) PA-8900 800MHz-1.1GHz with 1.5MB/1.5MB on-chip I/D L1 cache and 64MB off-chip L2 cache each

It is supposedly possible to upgrade the CPUs to Itanium/IA64 processors, since the integrated system chipset (zx1) chipset can support IA64 processors too.

Chipset

- HP zx1 Chipset (same as in Itaniums systems)
- 8MB Flash EEPROM
- Two-channel Ultra-320 SCSI controller
- UltraATA-133 IDE controller

Buses

- Itanium 2 memory/system bus
- PCI-X 64/133 I/O bus
- PCI-X 64/66 I/O bus
- PCI 64/33 I/O bus
- PCI 32/33 I/O bus
- SCSI-3 Ultra320 (LVD) storage I/O bus
- UltraATA-133 IDE bus secondary storage I/O bus

Memory

- PC2100 registered ECC DDR-266 DIMMs
- Takes up to 4GB modules

- 8 slots
- 32GB maximum
- 8.5GB/s memory bandwidth
- 80ns memory latency

Expansion

- One PCI-X 64-bit/133MHz slot, full-length
- Two PCI-X 64-bit/66MHz slots, full-length
- One PCI 64-bit/33MHz slot, full-length
- Two PCI 32-bit/33MHz slots, half-length
- One AGP-8X pro slot (150W max power with auxiliary power connector)
- I/O-slots

```
TOP
1  [#########]               PCI-32/33, short PCI cards
2  [#########]               PCI-32/33, short PCI cards
3     [##############]       AGP-8X pro
4  [###################]     PCI-64/33, short and full-length cards
5  [###################]     PCI-64/66, short and full-length cards
6  [###################]     PCI-64/66, short and full-length cards
7  [###################]     PCI-64/133, short and full-length cards
BOTTOM
```

Drives

- Up to four internal 3.5" bays for Ultra320 LVD SCSI harddrives with 68-pin connector
- Up to two internal 3.5" bays for UltraATA-133 IDE harddrives
- Three half-heigth 5.25" bays for externally accessible SCSI (LVD or SE) or UltraATA-133 drives

4.21.3 External Connectors

- 2 DB9 male RS232C serial
- 5 USB 2.0 ports (two in front, three in rear)
- TP/RJ45 Gigabit Ethernet
- 4 phone jacks (microphone, headphones, line-in and line-out) on optional 16-bit audio card

4.21.4 References

- **HP Workstation c8000 Technical Reference Guide**[89] (PDF, 2.7MB)
- **HP c8000 data sheet**[90] (PDF, 400KB)

4.21.5 Operating Systems

- HP-UX: 11i TCOE and MTOE

4.21.6 Physical dimensions/Power

- 490*287*572mm height*width*depth
- rack-mounted: 5U height, 203*424*572mm width*depth
- 18.6kg net weight, 21.4kg fully loaded
- 871W max. power input (410W typical "workstation configuration")
- 4.4A max. RMS at 200V
- 8.7A max. RMS at 100V

[89] http://h20000.www2.hp.com/bc/docs/support/SupportManual/c00093136/c00093136.pdf
[90] http://www.hp.com/workstations/risc/c8000/c8000.pdf

4.22 HP 9000/D-Class and R-Class

4.22.1 Overview

Project names - uname

- D200/D300: Ultralight - 9000/801
- D210/D310: Ultralight - 9000/811
- D220: Ultralight - 9000/803
- D320: Ultralight - 9000/813
- D230: Ultralight - 9000/823
- D330: Ultralight - 9000/833
- D250/D350: Ultralight - 9000/821/831
- D260/D360: Ultralight - 9000/841/851
- D270/D370: Ultralight - 9000/861/871
- D280/D380: Ultralight - 9000/810/820
- D390: Ultralight - 9000/800
- R380: Ultralight - 9000/800
- R390: Ultralight - 9000/800

Introduction

- D200/D300, D210/D310, D250/D350: January 1996
- D220/D320, D230/D330: January 1997
- D260/D360: Mai 1996
- D270/D370: November 1996
- D280/D380: September 1997
- D390: July 1998
- R380/R390: September 1998

The D-Class *Ultralight* Series were Enterprise servers designed to be flexible, upgradable and scalable. Many different models were sold which could be upgraded within the series to another model, a heap of options existed for different parts of each system. They were designated to bring Mid-Range performance for an Entry-level price; some models are two-way SMP capable, supported CPUs range from 32-bit PA-7100LC to 64-bit PA-8200 and lots of expansion cards and drives are available.

The R-Class *Ultralight* servers (R380/R390) are the rack-mountable versions of their D-Class counterparts (D380/D390), while being technically almost identical, except some differences in the I/O and storage configuration.

Common aspects:

- heavy & massive casing
- noisy
- draw lots of electrical power
- LCD front panel display for error-codes and/or status indicators

The Ultralight servers had a unique naming convention:

- the first number after the "D", **2** or **3**, indicates the general type; D-Class servers were available in two different versions: the smaller D**2**x0 and the bigger D**3**x0.
- the latter numbers [**00, 10, ..., 90**] indicate the "internal" features, like CPU and chipset.
- the **R**380/**R**390 are basically D380/D390 in a rack-mountable case.

4.22.2 Internals

CPU

- Dx00: PA-7100LC 75MHz with 1KB on-chip I L1 and 256KB off-chip unified L1 cache
- Dx10: PA-7100LC 100MHz with 1KB on-chip I L1 and 256KB off-chip unified L1 cache
- Dx20: PA-7300LC 132MHz with 64/64KB on-chip I/D L1 (and 1MB off-chip unified I/D L2) cache
- Dx30: PA-7300LC 160MHz with 64/64KB on-chip I/D L1 (and 1MB off-chip unified I/D L2) cache
- Dx50: 1-2 PA-7200 100MHz with 256/256KB off-chip I/D L1 and 2KB on-chip "assist" L1 cache each
- Dx60: 1-2 PA-7200 120MHz with 1024/1024KB off-chip I/D L1 and 2KB on-chip "assist" L1 cache each
- Dx70: 1-2 PA-8000 160MHz with 512/512KB off-chip I/D L1 cache each
- Dx80/R380: 1-2 PA-8000 180MHz with 1024/1024KB off-chip I/D L1 cache each
- D390/R390: 1-2 PA-8200 240MHz with 2048/2048KB off-chip I/D L1 cache each

Notes

- Systems with PA-7100LC/PA-7300LC processors are not SMP capable
- The 1KB on-chip L1 cache on systems with a PA-7100LC is not really a true cache
- The 2KB on-chip "assist" cache on systems with a PA-7200 is not really a true cache
- Systems with a PA-7300LC processor feature an optional 1MB external L2 cache, provided through 2 SRAM modules
- Upgrading from one type of CPU to another mostly requires more than just changing the CPU board Have a look at the *D-Class and R-Class System Upgrade Guide* document (see below).

Chipset

- LASI ASIC, which features:
  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller
  - WD 16C522 compatible parallel
  - Harmony CD/DAT quality 16-bit audio
  - NS 16550A compatible serial
- PA-7200/PA-8000-models: 2 U2/Uturn-IOA BC Runway ports
- PA-7300LC-models: Phantom PseudoBC GSC+ port
- WAX ASIC, adds functionality missing in LASI, e.g. HIL, 2nd RS232 ...
- WAX EISA bus-adaptor, connects EISA to GSC
- Intel 82503 Ethernet transceiver, media auto-selection
- CS4215 or AD1849 programmable CODECs
- D3x0: NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
- D390/R380/R390: DEC 21140 Fast Ethernet controller

Buses

- On SMP-capable systems: Runway; CPU/memory bus
- GSC+ bus for the general system level I/O
- EISA expansion bus
- D3x0: SCSI-2 Fast-Wide high-voltage differential (HVD) bus for main storage I/O
- SCSI-2 Fast-Narrow single-ended bus for main storage I/O

Note: the Fast-Wide differential bus is optional on the D2x0 models.

Memory

- 72-pin ECC SIMMs.
- Look into the cpu/memory-boards illustrations on how to install RAM cards.

The required access-time of the RAM modules depends on the used CPU, systems with a PA-8x00 will need 50ns modules, those with PA-7200 and 7300LC can take up to 60ns and PA-7100LC-based models can take even slower modules.

Expansion

- D2x0:
  - One slot for a GSC/HSC (EISA formfactor) card
  - Two slots for EISA cards
  - Three slots for either GSC/HSC (EISA formfactor) or EISA cards
- D3x0:
  - One slot for a GSC/HSC (EISA formfactor) card
  - Three slot for EISA cards
  - Four slots for either GSC/HSC (EISA formfactor) or EISA cards
- R380/R390:
  - One slot for a GSC/HSC (EISA formfactor) card
  - Four slot for EISA cards
  - Three slots for either GSC/HSC (EISA formfactor) or EISA cards
- See GSC expansion-cards
- See EISA expansion-cards

Drives

- D2x0/R3x0: Up to two Fast-Narrow 50-pin SCSI-2 single-ended harddrives
- D3x0: five hot-swap trays for a Fast-Wide 68-pin SCSI-2 high-voltage differential harddrive
- D-Class: Up to three 5.25 inch 50-pin Fast-Narrow SE SCSI half-height drives, external accessible
- R3x0: On 5.25 inch 50-pin Fast-Narrow SE SCSI half-height drive, external accessible

Note: If the Fast-Wide differential SCSI option exists on a D2x0, two optional trays for FWD drives are available.

4.22.3 External Connectors

- 50-pin HD SCSI-2 single-ended
- TP/RJ45 10BaseT 10Mbit Ethernet
- 2 DB9 male RS232C serial, one for console, one for USV
- DB25 female parallel
- 2 PS/2 connectors for keyboard und mouse

4.22.4 ROM update

There is a firmware update available for the D210 and D310 which contains the latest version (*38.43*).

- **PF_CULL3843.txt**[91] has details about the contents and installation of the patch.
- **PF_CULL3843**[92] contains the patch.

There is also a firmware update available for the D220, D230, D320 and D310 which contains the latest version (*38.46*).

- **PF_CULD3846.txt**[93] has details about the contents and installation of the patch.
- **PF_CULD3846**[94] contains the patch.

There is also a firmware update available for the D250, D260, D350 and D360 which contains the latest version (*36.34*).

- **PF_CULT3634.txt**[95] has details about the contents and installation of the patch.
- **PF_CULT3634**[96] contains the patch.

There is also a firmware update available for the D270, D280, D370, D380 and R380 which contains the latest version (*42.11*).

- **PF_CULU4211.txt**[97] has details about the contents and installation of the patch.
- **PF_CULU4211.frm**[98] contains the patch.

There is also a firmware update available for the D390 and R390 which contains the latest version (*42.10*).

- **PF_CULV4210.txt**[99] has details about the contents and installation of the patch.
- **PF_CULV4210.frm**[100] contains the patch.

4.22.5 References:

- **D-Class and R-Class Installation Guide**[101] (PDF, 0.4MB)
- **D-Class and R-Class Operator's Guide**[102] (PDF, 1.1MB)
- **D-Class and R-Class System Upgrade Guide**[103] (PDF, 0.9MB)
- **D-Class Entry Server description**[104] (PDF, HP Journal 7/97)

[91] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULL3843.txt
[92] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULL3843
[93] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULD3846.txt
[94] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULD3846
[95] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULT3634.txt
[96] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULT3634
[97] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULU4211.txt
[98] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULU4211.frm
[99] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULV4210.txt
[100] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CULV4210.frm
[101] http://docs.hp.com/hpux/pdf/A3262-90057.pdf
[102] http://docs.hp.com/hpux/pdf/A3262-90013.pdf
[103] http://docs.hp.com/hpux/pdf/A3262-90010.pdf
[104] http://www.hpl.hp.com/hpjournal/97jun/jun97a10.pdf

4.22.6 Operating Systems

- HP-UX: every 32-bit release from 10.20 - 11.11 works. Systems with a 64-bit PA-8x00 CPU also can use 64-bit version of HP-UX 11.x.
  - 10.20 for 800s servers: runs nicely.
  - 11.00 and 11i: run nicely.
- Linux: works.
- **D220/230, D320/330 only:** OpenBSD works.

4.22.7 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp
Dx00	115	146	2.18	2.90	19.2	25.8
Dx10	152	194	3.74	4.08	33.6	36.7
Dx20			6.57	6.72	59.2	60.5
Dx30			7.87	7.58	70.8	68.3
Dx50	144	218	5.01	6.77	45.1	61.0
Dx60						
Dx60					114	143
Dx70			10.40	15.00	93.9	135
Dx70 2-CPU					184	190
Dx80			12.30	17.40	111	157
Dx80 2-CPU					219	221
D390			15.50	25.50		

4.23 HP 9000/E-Class

4.23.1 Overview

Project names - uname(1):

- E25: Wright Brothers Orville - 9000/806
- E35: Wright Brothers Wilbur - 9000/816
- E45: Wright Brothers - 9000/826
- E55: Wright Brothers 96 - 9000/856

These were the low-cost UNIX server systems from HP in the mid-90s and the designated replacement for the older PA-7100-based F and G-Class Servers. Designed for reduced manufacturing cost, they were simultaneously developed with the 712 series systems. The casing was taken over almost unchanged from the F-Class, the CPU-board was a complete new design. Noteably only the LAN and several other functionality was utilized from the LASI chipset; due to time problems, a modified version of the F-Class HP-PB "Personality" (chipset) card was used for SCSI, serial MUX and parallel.

4.23.2 Internals

CPU

- E25: PA-7100LC 48MHz with 1KB on-chip I L1 *(See Note 1)* and 64KB off-chip unified I/D L1 cache
- E35: PA-7100LC 64MHz with 1KB on-chip I L1 *(See Note 1)* and 256KB off-chip unified I/D L1 cache
- E45: PA-7100LC 80MHz with 1KB on-chip I L1 *(See Note 1)* and 256KB off-chip unified I/D L1 cache
- E55: PA-7100LC 96MHz with 1KB on-chip I L1 *(See Note 1)* and 1024KB off-chip unified I/D L1 cache

Notes

1. The 1KB on-chip L1 cache is not really a true cache.

Chipset

- LASI ASIC
- WAX ASIC
- GSC-to-HP-PB bridge
- Several HP ASICs, controlling the HP-PB SCSI and MUX port

Buses

- GSC; system level I/O bus
- HP-PB; additional I/O bus
- SCSI-2 Fast-Narrow single-ended bus; main storage I/O

Memory

- 72-pin ECC SIMMs
- Takes 8-64MB modules
- 8 slots
- 16MB (2*8) minimum, 512MB (8*64) maximum

Expansion

- Two slots for HP-PB cards

Drives

- One tray for two 3.5" Fast-Narrow SE 50-pin SCSI harddrives
- One tray for three half-height 5.25" Fast-Narrow SE 50-pin drives, externally accessible

4.23.3 External Connectors

- 50-pin HD SCSI-2 single-ended
- high-pin-count MUX connector
- TP/RJ45 10Mbit Ethernet *(See Note 1)*
- 15-pin AUI 10Mbit Ethernet *(See Note 1)*
- DB25 female parallel

Notes

1. The system automatically detects the used port.

4.23.4 ROM update

There is a firmware update available for the E25, E35 and E45, which contains the latest version (*1.3*).

- **PF_CWBR0013.txt**[105] has details about the contents and installation of the patch.
- **PF_CWBR0013**[106] contains the patch.

[105] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CWBR0013.txt
[106] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CWBR0013

4.23.5 References

- **Development of a Low-Cost, High-Performance, Multiuser Business Server System**[107] (PDF, HP Journal 4/95)

4.23.6 Operating Systems

- HP-UX: every 32-bit release from 10.20 - 11.00 works.
  - 10.20 for 800s servers: runs nicely.
  - 11.00: runs nicely.
  - 11i: officially unsupported but some releases work. Faster than 11.00 on the same hardware.
- Linux: works, but the hardware support for the E-class is very limited, i.e. the SCSI-subsystem does not work.
- NetBSD: experimental support as of 5/2005, however some I/O-devices are not supported (e.g. SCSI).

4.23.7 Benchmarks

Model	SPEC92, int	SPEC92, fp
E25	45.0	66.7
E35	65.6	98.5
E45	82.1	122.9
E55	108.0	163.4

[107] http://www.hpl.hp.com/hpjournal/95apr/apr95a9.pdf

4.24 HP 9000/Nova Servers

4.24.1 Overview

Project names - uname

- F10: Nova8 - 9000/807
- F20: Nova Low - 9000/817
- F30: Nova High - 9000/837
- G30/H30: Nova High - 9000/847
- G40/H40: Nova64 - 9000/867
- G50/H50: TNova - 9000/887
- G60/H60: TNova96 - 9000/887
- G70/H70: Hydra96 - 9000/887
- H20: Nova Low - 9000/827
- I30: Nova High - 9000/857
- I40: Nova64 - 9000/877
- I50: TNova - 9000/897
- I60: TNova96 - 9000/897
- I70: Hydra96 - 9000/897

Introduction

- F-Class: January 1993
- G/H/I-Class: August 1991

The *Nova* Servers were the second-generation PA-RISC based servers from HP, released around 1990. They were available in many different sizes with different expansion options, CPU types and CPU frequencies. But all have several aspects in common:

- heavy & massive casing
- noisy
- draw *lots* of electrical power
- four status LEDs at front-panel
- no video output – serial console on a MUX-panel or mini-DIN
- are very cheap to get now.

All Nova servers had a unique naming convention:

- the front letter [**F, G, H, I**] indicates the "external" features, like casing and expansion,
- the latter number [**10, 20, ..., 70**] indicates the "internal" features, like CPU and chipset.

4.24.2 Internals

CPU

- F10: PA-7000 32MHz with 32/64KB off-chip I/D L1 cache
- *20: PA-7000 48MHz with 64/64KB off-chip I/D L1 cache
- *30: PA-7000 48MHz with 256/256KB off-chip I/D L1 cache
- *40: PA-7100 64MHz with 256/256KB off-chip I/D L1 cache
- *50: PA-7100 96MHz with 256/256KB off-chip I/D L1 cache
- *60: PA-7100 96MHz with 1024/1024KB off-chip I/D L1 cache
- *70: 1-2 PA-7100 96MHz with 2048/2048KB off-chip I/D L1 cache each

On systems with an PA-7000 the FPU was an optional add-on chip, so there is often an empty socket on the CPU-boards of these system.

Chipset

Based upon lots of HP custom ASICs with odd names, almost the whole peripheral-I/O is realized with HP-PB cards and so called "Personality Boards". There exists nearly nil documentation on the internals of these old systems, besides some code snippets in Mach/Lites 4.4 for PA-RISC. This renders any efforts to port a modern, "open" operating system to this platform more or less unrealistic, since no qualified documentation is freely available or expected to become so in the future.

Buses

- HP-PB bus for the general I/O
- SCSI-2 Narrow single-ended bus for main storage I/O

Memory

- HP proprietary modules
- 12 slots
- ? minimum, 768MB (12*64MB) maximum

Expansion

- F*: 2 HP-PB slots
- G*: 4 HP-PB slots
- H*: 8 HP-PB slots
- I*: 12 HP-PB slots

Drives

- ? (lots)

4.24.3 External Connectors

- 50-pin HD SCSI-2 single-ended
- high-pin-count MUX connector
- DB25 female parallel
- rest depends on installed HP-PB cards

4.24.4 References

- Pinout for the mini-DIN console connector at the back

4.24.5 Operating Systems

The only operating system that runs on these servers is HP-UX; all of these servers are officially supported in versions 10.20 for 800s servers and 11.00. Official support for the Nova servers was dropped in 11.11 (11i), however it is still possible in most cases to install and run 11i on these systems, although the OS patches must be carefully reviewed as some could very well break the system (e.g. patches to the SCSI-subsystem).

4.24.6 Benchmarks

Model	SPEC92, int	SPEC92, fp
F10	22.0	36.6
*20	33.6	56.1
*30	37.8	62.4
*40	65.2	91.3
*50	100.0	158.5
*60	108.8	195.3
*70	108.8	195.3

All results are for single-CPU systems.

4.25 HP 9000/J-Class

4.25.1 Overview

Project names - uname(1):

- J200: Skyhawk - 9000/770
- J210: Skyhawk - 9000/770
- J210XC: Light Hawk - 9000/770
- J280: Firehawk - 9000/780
- J282: Firehawk - 9000/780
- J2240: SummitHawk - 9000/782

The J-Class are powerful, SMP-capable and well expandable PA-RISC workstations. They feature a deskside chassis with four interlocked modules, which you can take out easily for maintenance. The J280 is only a single-processor machine, which can be upgraded to a dual-capable J282. This requires at least changing the mainboard.

4.25.2 Internals

CPU

- J200: 1-2 PA-7200 100MHz with 256/256KB off-chip I/D L1 and 2KB on-chip "assist" L1 cache
  - 64-bit wide bus to cache
  - 800MB/s I-fetch (8-Byte)
  - 800MB/s D-load (16-Byte), 800MB/s single D-store (8-Byte)
- J210: 1-2 PA-7200 120MHz with 256/256KB off-chip I/D L1 and 2KB on-chip "assist" L1 cache
  - 64-bit wide bus to cache
  - 960MB/s I-fetch (8-Byte)
  - 960MB/s D-load (16-Byte), 960MB/s single D-store (8-Byte)
- J210XC: 1-2 PA-7200 120MHz with 1/1MB off-chip I/D L1 and 2KB on-chip "assist" L1 cache
  - 64-bit wide bus to cache
  - 960MB/s I-fetch (8-Byte)
  - 960MB/s D-load (16-Byte), 960MB/s single D-store (8-Byte)
- J280: 1 PA-8000 180MHz with 1/1MB off-chip I/D L1 cache
  - 128-bit wide bus to cache
  - 2.88GB/s I-fetch
  - 2.88GB/s D-load (16-Byte), 1.44GB/s D-store (8-Byte)

- J282: 1-2 PA-8000 180MHz with 1/1MB off-chip I/D L1 cache
  - 128-bit wide bus to cache
  - 2.88GB/s I-fetch
  - 2.88GB/s D-load (16-Byte), 1.44GB/s D-store (8-Byte)
- J2240: 1-2 PA-8200 236MHz with 2/2MB external I/D L1 cache

The 2KB on-chip "assist" cache is not really a true cache.

Chipset

- LASI ASIC, which features:
  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller
  - WD 16C522 compatible parallel
  - Harmony CD/DAT quality 16-bit stereo audio
  - NS 16550A compatible serial
- Two U2/Uturn-IOA BC Runway ports
- WAX ASIC, adds functionality missing in LASI, e.g. HIL, 2nd RS232 ...
- WAX EISA bus-adaptor, connects EISA to GSC
- Intel 82C503 Ethernet transceiver, media auto-selection
- CS4215 or AD1849 programmable CODECs
- NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
- J2240: Dino GSC-to-PCI bridge
- J2240: Cujo GSC-to-PCI bridge
- J2240: Symbios Logic 53C895 16-bit Ultra-Wide SCSI-2 controller
- J2240: DEC 21142/43 (*Tulip*) Fast-Ethernet controller

Buses

- Runway; CPU/memory bus
- GSC; system level I/O bus
- EISA; additional expansion I/O bus
- SCSI-2 Fast-Wide *high-voltage differential* bus; main storage I/O
- SCSI-2 Fast-Narrow single-ended bus
- J2240: SCSI-3 Ultra-Wide single-ended bus; main storage I/O
- J2240: PCI bus;

Memory

- 72-pin ECC SIMMs, 60ns or faster
- Bus width: 128 data bits with 16 check bits
- Up to 8-way interleaving
- J200: 800MB/s peak bandwidth
- J210[XC]: 960MB/s peak bandwidth
- Take 16-128MB modules (needs latest firmware-rev)
- 16 slots
- 32MB (2*16) minimum, 2GB (16*128) maximum
- J2240: 4GB maximum (with 256MB modules)

Expansion

- One slot for a GSC (*EISA formfactor*) card
- Two slots for EISA cards
- Two slots for either GSC (*EISA formfactor*) or EISA cards
- Slot layout:

```
TOP
4:  [##########]              - EISA
3:  [##########]              - EISA
2:  [##########]       [#####] - EISA or GSC
1:  [##########]       [#####] - EISA or GSC
0:                     [#####] - GSC (for primary graphics)
BOTTOM
```

- See GSC expansion-cards
- See EISA expansion-cards

J2240:

- One slot for a PCI 32-bit/33MHz, 5V card
- One slot for either a PCI 32-bit/33MHz, 5V or EISA card
- One slot for either a GSC or PCI 32-bit 32-bit/33MHz, 5V card
- Two slots for either GSC or PCI 64-bit/66MHz, 3.3V cards
- Slot layout:

```
TOP
4:     [#####]                - PCI-32/33, 5V or
```

```
    [##########]              - EISA
3:     [#####]                - PCI-32/33, 5V
2:     [#########]     [#####] - PCI-64/66, 3.3V or GSC
1:     [#####]         [#####] - PCI-32/33, 5V or GSC
0:     [#########]     [#####] - PCI-64/66, 3.3V or GSC (for primary graphics)
BOTTOM
```

Drives

- One tray for two 3.5" Fast-Wide HVD 68-pin SCSI harddrives
- One tray for two half-heigth 5.25" Fast-Narrow SE 50-pin SCSI drives, external accessible

4.25.3 External Connectors

- 50-pin HD SCSI-2 Fast-Narrow single-ended
- 68-pin HD SCSI-3 Fast-Wide *high-voltage differential* (HVD)
- J2240: 68-pin HD SCSI-3 Ultra-Wide single-ended
- 2 DB9 male RS232C serial (up to 460.8Kb/s)
- DB25 female parallel
- TP/RJ45 10Mbit Ethernet /
- J2240: TP/RJ45 10/100Mbit Ethernet
- 15-pin AUI 10Mbit Ethernet
- Graphics port depends on installed framebuffer
- 2 PS/2 connectors for keyboard & mouse
- HP-HIL for input device loop
- 4 phone jacks (microphone, headphones, line-in and ?)

4.25.4 ROM update

There is a firmware update available for the J200 & J210, which contains the latest version (*2.0*).

- **PF_CJ2X0020.txt**[108] has details about the contents and installation of the patch.
- **PF_CJ2X0020**[109] contains the patch.

There is also a firmware update available for the J280 & J282, which contains the latest version (*2.5*).

- **PF_CJ28X025.txt**[110] has details about the contents and installation of the patch.

[108] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CJ2X0020.txt
[109] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CJ2X0020
[110] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CJ28X025.txt

- **PF_CJ28X025**[111] contains the patch.

There is also a firmware update available for the J2240, which contains the latest version (*2.1*).

- **PF_CJ224021.txt**[112] has details about the contents and installation of the patch.
- **PF_CJ224021**[113] contains the patch.

4.25.5 References

- **Visualize J200, J210 technical reference manual**[114] (PDF, 2.6MB)
- **Visualize J280 Owner's Guide**[115] (PDF, 6.3MB)
- **Visualize J280 workstation upgrade instructions**[116] (PDF, 1.9MB)
- **Visualize J280, J282, J2240 Service Handbook**[117] (PDF, 6.8MB)
- **Visualize J282, J2240 Owner's Guide**[118] (PDF, 3.1MB)
- **Visualize J282 workstation upgrade instructions**[119] (PDF, 2.3MB)
- **Visualize J2240 workstation upgrade instructions**[120] (PDF, 1MB)
- **Replacing the EEPROM on an HP Visualize J282**[121] (HTML). In case your J-Class needs a new EEPROM chip (which is the case if it displays

```
FLT  3004
     PDH
```

  on its LCD display).
- **J/K-Class Memory System description**[122] (PDF, HP Journal 2/96)

4.25.6 Operating Systems

- HP-UX: every 32-bit release from 10.20 - 11.11 works.
  - 10.20: runs very nicely.
  - 11.00 and 11i: run nicely. You need *EP9808* to run a 64-bit 11.0 environment on a machine with a 64-bit PA-8000
- Linux: works fine.
- J200, J210: OpenBSD works, although the FWD SCSI-controller is not supported.

[111] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CJ28X025
[112] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CJ224021.txt
[113] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CJ224021
[114] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37962/lpv37962.pdf
[115] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37675/lpv37675.pdf
[116] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv38001/lpv38001.pdf
[117] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37964/lpv37964.pdf
[118] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37966/lpv37966.pdf
[119] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37965/lpv37965.pdf
[120] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37963/lpv37963.pdf
[121] http://www.lava.net/~kirill/j282/eeprom.html
[122] http://www.hpl.hp.com/hpjournal/96feb/feb96a5.pdf

4.25.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPECrate95, int	SPECrate95, fp
J200	4.98	4.50	44.8	61.3
J200 2-CPU			64.5	105
J210	6.00	5.40	54.0	73.4
J210 2-CPU			77.5	126
J210XC	6.40	5.70	57.6	81.5
J210XC 2-CPU			82.8	142
J280	11.80	19.30		
J282	?	?		
J2240	17.40	26.30	157	237
J2240 2-CPU			307	349

4.25.8 Physical dimensions/Power

- 470*330*541mm height*width*depth
- 36kg net weight, 49.9kg fully loaded
- 1150W max. power input
- 6A max. RMS at 240V
- 12A max. RMS at 120V

4.26 HP Visualize J5x00 and J7x00

4.26.1 Overview

Project names/uname(1):

- J5000: Forte 2W - 9000/785
- J5600: Forte W+ 2W - 9000/785
- J7000: Forte 4W - 9000/785
- J7600: Forte W+ 4W - 9000/785

These workstations were aimed at the graphics workstations market, equipped with up to two 64-bit PA-8500 featuring large on-chip L1 caches. They are basically the bigger brothers of the C3000/C3600 et al, featuring better expandability. The architecture was a major change from those of its predecessors, e.g. the C200 et al. New I/O devices were integrated, the LASI I/O chip was dumped, together with the GSC bus. All device I/O now sits on various PCI buses, human I/O devices are connected to USB ports. The case also was a major redesign.

4.26.2 Internals

CPU

- J5000: 1-2 PA-8500 440MHz with 512/1024KB on-chip I/D L1 cache each
- J5600: 1-2 PA-8600 552MHz with 512/1024KB on-chip I/D L1 cache each
- J7000: 1-4 PA-8500 440MHz with 512/1024KB on-chip I/D L1 cache each
- J7600: 1-4 PA-8600 552MHz with 512/1024KB on-chip I/D L1 cache each

Chipset

- Astro memory/Runway controller
- 4 Elroy PCI bridges
- National 87560 *(SuperI/O)*, handling USB, RS232, parallel, floppy and IDE
- National 87415 IDE controller
- National USB controller
- Analog Devices AD1889 sound chip
- DEC 21142/43 Fast Ethernet controller *(Tulip)*
- Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

- Runway; CPU/memory bus
- PCI-64/33; high-performance device I/O bus

- PCI-64/66; high-performance graphics I/O bus
- SCSI-2 Ultra-Narrow single-ended bus
- SCSI-3 Ultra2-Wide LVD bus; main storage I/O
- IDE bus; CD/floppy I/O

Memory

- 278-pin 120MHz ECC SDRAM DIMMs
- Takes 256/512/1024MB modules
- J5000: 8 slots
- J7000: 16 slots
- 256MB (1*256) minimum, J5000: 8GB (8*1024) maximum; J7000: 16GB (16*1024) maximum.

Expansion

- Five PCI 64-bit/33MHz, 5V slots
- Two PCI 64-bit/66MHz, 3.3V slots
- I/O-slots

```
TOP
1  EMPTY
2  [##################]       PCI-64/33, 5V
3  [##################]       PCI-64/33, 5V
4  [##################]       PCI-64/66, 3.3V
5  [##################]       PCI-64/33, 5V
6  [##################]       PCI-64/33, 5V
7  [##################]       PCI-64/66, 3.3V
8  [##################]       PCI-64/33, 5V
BOTTOM
```

Drives

- One tray for four 3.5" Ultra2-Wide LVD SCSI harddrives with 80-pin SCA connector
- One tray for a 3.5" Floppy drive
- One tray for a half-heigth 5.25" SCSI drive, external accessible

4.26.3 External Connectors

- 50-pin HD SCSI-2 Ultra-Narrow single-ended
- 68-pin HD SCSI-3 Ultra2-Wide LVD
- 2 DB9 male RS232C serial

- DB25 female parallel
- TP/RJ45 10/100Mbit Ethernet
- 2 USB ports for keyboard & mouse
- 4 phone jacks (microphone, headphones, line-in and line-out)

4.26.4 ROM update

There is an firmware update available which contains the latest version (*5.0*).

- **PF_CBCJ0050.txt**[123] has details about the contents and installation of the patch.
- **PF_CBCJ0050**[124] contains the patch.

4.26.5 References

- **J5x00/J7x00 Owner's Guide**[125] (PDF, 4.5MB)
- **J5x00/J7x00 Service Handbook**[126] (PDF, 4.4MB)
- **VISUALIZE Workstation Memory Subsystem**[127] (PDF, 120KB)

4.26.6 Operating Systems

- HP-UX: every release from 10.20 *ACE 9907* - 11.11 works.
  - 10.20: very fast You need at least *ACE 9907*.
  - 11.00 and 11i: run nicely. You need at least 11.0 *ACE 9911* or 11i.
- Linux: works.

4.26.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp	SPEC2000, int	SPEC2000, fp
J5000	32.50	54.00	302	486		
J5000 2-CPU			579	744		
J5600	42.60	62.70	384	564	408	392
J5600 2-CPU			758	847		
J7000	32.50	54.00	302	486		
J7000 2-CPU			579	744		

[123] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050.txt
[124] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050
[125] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37967/lpv37967.pdf
[126] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37674/lpv37674.pdf
[127] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37826/lpv37826.pdf

4.27 HP Visualize J6000, J6700

4.27.1 Overview

Project names - uname(1):

- J6000: Duet W+ - 9000/785
- J6700: Duet W2 - 9000/785
- J6750: Duet W2 - 9000/785

These small workstations were aimed at the graphics workstations market, equipped with the new 64-bit PA-8600 and PA-8700, both featuring large on-chip L1 caches. The architecture was a major change from those of its predecessors. New I/O-devices were integrated, the LASI I/O chip was dumped together with the old GSC bus. All these devices now sit on several PCI buses, human I/O devices are connected to USB ports. The very small case can be used on the desktop or fitted in a 19"-rack.

4.27.2 Internals

CPU

- J6000: 1-2 PA-8600 552MHz with 512/1024KB on-chip I/D L1 cache
- J6700: 1-2 PA-8700 750MHz with 768/1536KB on-chip I/D L1 cache
- J6750: 1-2 PA-8700+ 875MHz with 768/1536KB on-chip I/D L1 cache

Chipset

- Astro memory/Runway controller
- 4 Elroy PCI bridges
- National 87560 (SuperI/O), handling USB, RS232, parallel, floppy and IDE
- National 87415 IDE controller
- National USB controller
- Analog Devices AD1889 sound chip
- DEC 21142/43 Fast Ethernet controller *(Tulip)*
- Symbios Logic 53C896 Ultra2-Wide SCSI-3 controller

Buses

- Runway; CPU/memory bus
- PCI-64/33; high-performance device I/O bus
- PCI-64/66; high-performance graphics I/O bus
- SCSI-2 Ultra-Narrow single-ended bus
- SCSI-3 Ultra2-Wide LVD buses; main storage I/O
- IDE bus; CD-I/O

Memory

- 278-pin 120MHz ECC SDRAM DIMMs
- 16 slots
- Takes 512MB/1GB DIMMs
- 1GB (2*512) minimum, 16GB maximum (16*1G)

Expansion

- Three PCI 64-bit/66MHz, 3.3V slots

Drives

- One tray for two 3.5" Ultra2-Wide LVD SCSI harddrives with 80-pin SCA connector
- One tray for a slim-line ATAPI CD-ROM

4.27.3 External Connectors

- Combined 50-pin HD SCSI-2 Ultra-Narrow single-ended and 68-pin HD SCSI-3 Ultra2-Wide LVD connector (?)
- two DB9 male RS232C serial
- DB25 female parallel
- TP/RJ45 10/100Mbit Ethernet
- two USB ports for keyboard & mouse
- four phone jacks (microphone, headphones, line-in and line-out)

4.27.4 ROM update

There is a firmware update available for the **PA-8600**-based J6000, which contains the latest version (*5.0*).

- **PF_CBCJ0050.txt**[128] has details about the contents and installation of the patch.
- **PF_CBCJ0050**[129] contains the patch.

A different firmware update is provided for the **PA-8700**-based J67x0 systems (version 2.0):

- **PF_CCJ70020.txt**[130] has details about the contents and installation of the patch.
- **PF_CCJ70020**[131] contains the patch.

[128] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050.txt
[129] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CBCJ0050
[130] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CCJ70020.txt
[131] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CCJ70020

4.27.5 References

- **J6000 Service Handbook**[132] (PDF, 4.5MB)
- **J6000 Technical Reference**[133] (PDF, 3.3MB)
- **J6700 Service Handbook**[134] (PDF, 9.8MB)
- **J6700 Technical Reference**[135] (PDF, 5.6MB)

4.27.6 Operating Systems

- HP-UX:
  - J6000: HP-UX 10.20: runs, need ACE 9907
  - 11.00 and 11i: run nicely. You need at least 11.0 *ACE 9911* or 11i.
- Linux: works.

4.27.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPEC95rate, int	SPEC95rate, fp	SPEC2000, int	SPEC2000, fp
J6000	42.60	62.70	384	564	408	392
J6000 2-CPU			758	847		
J6700	57.60	85.90			469	526

[132] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37677/lpv37677.pdf
[133] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37634/lpv37634.pdf
[134] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37640/lpv37640.pdf
[135] http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37641/lpv37641.pdf

4.28 HP 9000/K-Class

4.28.1 Overview

Project names - uname

- K100: Kittyhawk - 9000/809
- K200: Kittyhawk - 9000/819
- K210: Kittyhawk - 9000/839
- K220: Thunderhawk - 9000/859
- K250: Mohawk - 9000/802
- K260: Mohawk - 9000/879
- K370: Bravehawk - 9000/898
- K380: Dragonhawk U+ - 9000/800
- K400: Kittyhawk - 9000/829
- K410: Kittyhawk - 9000/849
- K420: Thunderhawk - 9000/869
- K450: Mohawk - 9000/804
- K460: Mohawk - 9000/889
- K570: Bravehawk - 9000/899
- K580: Dragonhawk U+ - 9000/800

Introduction

- Kx00: March 1995
- Kx10: September 1995
- Kx20: March 1996
- Kx50, K260: August 1996
- K360/K460: June 1998
- Kx70: Mai 1997
- Kx80: February 1998

All K-Class systems except the K100 are multiprocessor systems. The K370/K380 and K570/K580 are able to support up to 6-way multiprocessing, whereas the K2x0 and K4x0 support up to 4-way multiprocessing. A typical K-Class server consists of a *System Processing Unit* (SPU), system console and an optional *Uninterruptible Power Supply* (UPS). These units then are packaged in a 19-inch rack. It is also possible to use the SPU itself without the UPS and the attached system-console.

- The first number after the "K", **1**, **2**, **3**, **4** or **5** indicates the general type:

  - a K100 is a single-CPU system with limited expandability,
  - a K2x0 takes up to four CPUs, has better expandability (more RAM) than a K100,
  - a K3x0 takes up to six CPUs, has more I/O-slots than a K2x0,
  - a K4x0 takes up to four CPUs, has more I/O-slots and supports partially more RAM than a K2x0,
  - a K5x0 takes up to six CPUs, has a different I/O-configuration than a K3x0.
- The latter numbers [**00, 10, ..., 80**] indicate the "internal" features, like CPU and chipset.

4.28.2 Internals

CPU

- K100: PA-7200 100MHz with 256/256KB off-chip I/D L1 and 2KB on-chip "assist" L1 cache
- K200/K400: 1-4 PA-7200 100MHz with 256/256KB off-chip I/D L1 and 2KB on-chip "assist" L1 cache each
- K210/K410: 1-4 PA-7200 120MHz with 256/256KB off-chip I/D L1 and 2KB on-chip "assist" L1 cache each
- K220/K420: 1-4 PA-7200 120MHz with 1024/1024KB off-chip I/D L1 and 2KB on-chip "assist" L1 cache each
- K250/K450: 1-4 PA-8000 160MHz with 1024/1024KB off-chip I/D L1 cache each
- K260/K460: 1-4 PA-8000 180MHz with 1024/1024KB off-chip I/D L1 cache each
- K370/L570: 1-6 PA-8200 200MHz with 2048/2048KB off-chip I/D L1 cache each
- K380/K580: 1-6 PA-8200 240MHz with 2048/2048KB off-chip I/D L1 cache each

The 2KB on-chip "assist" cache on systems with a PA-7200 is not really a true cache.

Chipset

- LASI ASIC, which features:
  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller
  - WD 16C522 compatible parallel
  - Harmony CD/DAT quality 16-bit stereo audio
  - NS 16550A compatible serial
- 2 U2/Uturn-IOA BC Runway ports
- Gecko BOA BC GSC+ Port
- Intel 82503 Ethernet transceiver, media auto-selection
- CS4215 or AD1849 programmable CODECs
- NCR 53C720 16-bit Fast-Wide *high-voltage differential* (HVD) SCSI-2
- Eole CAP/MUX

Buses

- Runway; CPU/memory bus
- GSC+ bus for the general system level I/O
- HSC bus for expansion I/O
- HP-PB bus for expansion I/O
- SCSI-2 Fast-Wide high-voltage differential (HVD) bus for main storage I/O
- SCSI-2 Fast-Narrow single-ended bus for main storage I/O

Memory

- 72-pin ECC SIMMs on special RAM-boards.

The required access-time of the RAM modules depends on the used CPU in the system, systems with a PA-8x00 need 50ns modules, those with PA-7200 and can take up to 60ns. It is possible that slower modules will also work.

Expansion

K100/K2x0:

- One slot for a GSC/HSC (HSC formfactor) card on the core-I/O board
- Four slots for HP-PB cards, from which two slots can either be used for single or double-height HP-PB cards.

K3x0:

- One slot for a GSC/HSC (HSC formfactor) card on the core-I/O board
- Through the use of an 2-slot HSC I/O-expansion module, which can be installed at the rear into the slot right of the core-I/O, these models can faciliate two more GSC/HSC (HSC formfactor) cards.
- Four slots for HP-PB cards, from which two slots can either be used for single or double-height HP-PB cards.

K4x0:

- One slot for a GSC/HSC (HSC formfactor) card on the core-I/O board
- Through the use of an 2 or 4-slot HSC I/O-expansion module, which can be installed at the rear into the slot right of the core-I/O, these models can faciliate two or four more GSC/HSC (HSC formfactor) cards.
- Eight slots for HP-PB cards, from which four slots can either be used for single or double-height HP-PB cards.

K5x0:

- One slot for a GSC/HSC (HSC formfactor) card on the core-I/O board
- Through the use of an 2 or 4-slot HSC I/O-expansion module, which can be installed at the rear into the slot right of the core-I/O, these models can faciliate two or four more GSC/HSC (HSC formfactor) cards.
- Four slots for HP-PB cards, from which two slots can either be used for single or double-height HP-PB cards.

Drives

- One tray for four Fast-Wide 68-pin SCSI-2 high-voltage differential hard-drives
- one vertical tray for two 5.25 inch half-height drives, external accessible

4.28.3 External Connectors

- 68-pin HD SCSI-2 Fast-Wide high-voltage differential
- TP/RJ45 10BaseT 10Mbit Ethernet
- 15-pin AUI 10Mbit Ethernet
- two DB9 male RS232C serial, one for console, one for UPS
- DB25 male RS232C serial, for remote console via modem
- DB25 female parallel
- two PS/2 connectors for keyboard und mouse
- MDP-connector for a serial MUX
- Kx50/Kx60/Kx70/Kx80: four audio jacks

4.28.4 ROM update

There is a firmware update available for the K200, Kx10, Kx20 and K400 which contains the latest version (*2.9*).

- **PF_CKHK0029.txt**[136] has details about the contents and installation of the patch.
- **PF_CKHK0029**[137] contains the patch.

There is a firmware update available for the Kx50/Kx60 which contains the latest version (*39.43*).

- **PF_CMHK3943.txt**[138] has details about the contents and installation of the patch.
- **PF_CMHK3943**[139] contains the patch.

There is a firmware update available for the Kx60 which contains the latest version (*41.33*).

[136] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CKHK0029.txt
[137] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CKHK0029
[138] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CMHK3943.txt
[139] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CMHK3943

- **PF_CMHK4133.txt**[140] has details about the contents and installation of the patch.
- **PF_CMHK4133**[141] contains the patch.

4.28.5 References

- K-Class Front Panel Display Codes
- **Service Manual HP 9000 K-Class Enterprise Servers and HP 3000 Model 9x9KS**[142] (PDF, 2.1MB)
- **K-Class Installation Guide (HP 9000/Kxx0)**[143] (PDF)
- **K-Class Installation Guide (HP 3000/9x9KS)**[144] (PDF)
- **K-Class Owner's Guide**[145] (PDF)
- **K-Class System Upgrade Manual**[146] (PDF)
- **J/K-Class Memory System description**[147] (PDF, HP Journal 2/96)

4.28.6 Operating Systems

- HP-UX: every 32-bit release from 10.20 - 11.11 works. Systems with a 64-bit PA-8x00 CPU also can use 64-bit version of HP-UX 11.x.
  - 10.20 for 800s servers: runs very nicely.
  - 11.00 and 11i: run nicely
- Linux: works on most models.
- OpenBSD: on-going work to support at least the K220.

4.28.7 Benchmarks

Model	SPEC95, int	SPEC95, fp	SPECrate95, int	SPECrate95, fp
Kx00	4.92	6.80	44.3	61.2
Kx00 2-CPU			87.9	117
Kx00 4-CPU			174	198
Kx10	5.92	8.15	53.3	73.4
Kx10 2-CPU			106	140
Kx10 4-CPU			210	238
Kx20	6.41	9.11	57.7	82.0
Kx20 2-CPU			114	157
Kx20 4-CPU			228	275
Kx50	10.7	18.8	96.	169

[140] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CMHK4133.txt
[141] ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/PF_CMHK4133
[142] http://ftp.parisc-linux.org/docs/platforms/A2375-90004.pdf
[143] http://docs.hp.com/hpux/pdf/A2375-90006.pdf
[144] http://docs.hp.com/hpux/pdf/A2375-90005.pdf
[145] http://docs.hp.com/hpux/pdf/A2375-90003.pdf
[146] http://docs.hp.com/hpux/pdf/A2375-90011.pdf
[147] http://www.hpl.hp.com/hpjournal/96feb/feb96a5.pdf

Kx50 2-CPU			189	279
Kx50 4-CPU			375	383
Kx60	11.8	20.2	107	182
Kx60 2-CPU			212	297
Kx60 4-CPU			418	398
Kx70	14.6	23.0	132	207
Kx70 2-CPU			261	322
Kx70 4-CPU			519	434
Kx70 6-CPU			767	489
Kx80	17.4	28.5	157	257
Kx80 2-CPU			312	398
Kx80 4-CPU			610	532
Kx80 6-CPU			902	604

4.28.8 Physical dimensions/Power

Stand-alone:

- 635*432*698mm height*width*depth
- 59kg weight

Packaged:

- 870*889*775mm height*width*depth
- 76.66kg

Kx00/Kx10/Kx20:

- 1250W max. power input, 450W typical
- 6A max. RMS at 240V
- 10.5A max. RMS at 120V

Kx50/Kx60/Kx70:

- 2400W max. power input
- 10A max. RMS at 240V
- 16A max. RMS at 120V
- Require 20A power services.

4.29 RDI PrecisionBook

4.29.1 Overview

Project names:

- PrecisionBook 132
- PrecisionBook 160
- PrecisionBook 180

These portable workstations produced by **RDI (Tadpole)**[148] are essentially C132L/C160L workstations in a laptop case (which was used for other RDI computers as well, e.g. the UltraSPARC based laptops). The PrecisionBooks mostly use the same technology as the HP 9000 workstations with only some slight differences. A major difference to its desktop cousins is the integrated Cardbus controller for which Tadpole supplied a driver kit for use in HP-UX, although support for actual Carbus and PCMCIA devices was very sparse (NE2000-based Ethernet as an example). OpenBSD fully supports the Cardbus controller and a range of different Cardbus and PCMCIA devices (Fast-Ethernet, WLAN, etc).

4.29.2 Internals

CPU

- PrecisionBook 132: PA-7300LC 132MHz with 64/64KB on-chip I/D L1 (and 1MB off-chip unified I/D L2) cache
- PrecisionBook 160: PA-7300LC 160MHz with 64/64KB on-chip I/D L1 (and 1MB off-chip unified I/D L2) cache
- PrecisionBook 180: PA-7300LC 180MHz with 64/64KB on-chip I/D L1 (and 1MB off-chip unified I/D L2) cache

The external L2 cache is optional but was supplied with most systems.

Chipset

- LASI ASIC, which features:
  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller
  - WD 16C522 compatible parallel
  - Harmony CD/DAT quality 16-bit stereo audio
  - NS 16550A compatible serial
- Dino GSC-to-PCI bridge

[148] http://www.tadpolecomputer.com/html/

- Phantom PseudoBC GSC+ port
- Visualize-EG (*Graffiti*) graphics
- 1MB flash memory
- Intel 82503 Ethernet transceiver, media auto-selection
- CS4215 or AD1849 programmable CODECs
- WD37C65C Floppy controller
- 2 Cirrus CL-PD6832 PCI-CardBus bridges
- CMD PCI0643 IDE/UDMA33 controller

Display

- Either 12.1 (0.24mm dot pitch) or 14.1-inch (0.28mm dot pitch) active matrix LCD
- XGA resolution (1024x768)
- 16M colors plus 256 shades of gray
- 60Hz refresh
- External monitor output supports VGA, SVGA, XGA, SXGA and 1600x1200 resolutions at refresh rates of 60, 72 and 75Hz.
- At XGA-operation, both LCD and external CRT can be used simultaneously, if external CRT should display resolutions other than XGA, the LCD will be blanked.

Human Input

- PS/2-compatible, 97-key keyboard
- 3-button trackpad

Energy

- Lithium-Ionen battery with 40W/h capacity, 450g
- Runs about 0.5-1 hours
- Recharge time of 2.5 hours when system off
- Laptop draws about 70W continous, needs an input of 19V DC @ 3.68A from an AC-Adapter/Charger with non-standard pinout (though there are apparently some PrecisionBooks with a standard plug).

Buses

- GSC-2; general system-level I/O bus
- PCI-32/33; device I/O bus
- SCSI-2 Fast-Narrow single-ended bus; disk-I/O

- PDH bus, peripheral interface connecting to flash memory, NVRAM and PSM bus
- PSM bus, provides connection to the power-supply module

Memory

- Proprietary ECC modules, 60ns, 144-bit wide bus
- Takes 32-256MB modules, which utilize 16Mbit or 64Mbit DRAMs in either 1Mx16 or 4Mx16 configuration
- 2 slots
- 32MB (1*32) minimum, 512MB (2*256) maximum

Expansion

- Two Cardbus slots, supporting Cardbus and PCMCIA expansion cards

Drives

- Two trays for 2.5" IDE harddrives with SCSI-adapter (see below for more info) or for 2.5" SCSI drives

4.29.3 External Connectors

- 50-pin HD SCSI-2 single-ended
- TP/RJ45 10Mbit Ethernet
- VGA 15-pin Dsub graphics connector
- 2 PS/2 connectors for keyboard/mouse
- 4 phone jacks (microphone, headphones, line-in and ?)
- 15-pin connector for external floppy
- high-pin-count connector for dockingstation
- connector for an I/O breakout cable which provides:
  - 2 DB9 male RS232C serial
  - DB25 female parallel
  - AUI 10Mbit Ethernet

4.29.4 References

- **ADTX SCSI-IDE converters**[149] information
- **PrecisionBook hardware reference guide**[150] (PDF, 2.0MB)

[149] http://mickey.lucifier.net/adtx/
[150] ftp://ftp.tadpole.com/support/Precisionbook/Manuals/precisionbook-hardware-refguide.pdf

- **PrecisionBook user guide**[151] (PDF, 1.4MB)
- **RDI software for HP-UX 10.20 installation guide**[152] (PDF, 0.8MB)
- **RDI software release notes**[153] (PDF, 0.1MB)

4.29.5 Operating Systems

- HP-UX: every 32-bit release from 10.20 - 11.11 works.
  - 10.20: runs very nicely.
  - 11.00 and 11i: run nicely
- Linux: should work.
- NetBSD: should work.
- OpenBSD: works fine.

4.29.6 Benchmarks

Model	SPEC95, int	SPEC95, fp
PrecisionBook 132	6.49	6.54
PrecisionBook 160	7.78	7.39
PrecisionBook 180	9.22	9.43

[151] ftp://ftp.tadpole.com/support/Precisionbook/Manuals/precisionbook-hardware-userguide.pdf
[152] ftp://ftp.tadpole.com/support/Precisionbook/Manuals/hpux-10-2-installation-guide.pdf
[153] ftp://ftp.tadpole.com/support/Precisionbook/Manuals/rdi-software-release-notes.pdf

4.30 SAIC Galaxy 1100

4.30.1 Overview

This portable PA-RISC workstation built by **SAIC**[154] is a very rare system, originally build for purposedly military applications. It is has the following classifications:

- portable requirements: *Navy TAC-4*
- shock: *Federal Test Method Standard 101C, Method 5007.1 free-fall drop test*
- airborne: *MIL-STD-740-1, Grade C, Table 1*

It is fully software compatible to the HP 9000/700 range of systems and is technically just a 712 in a ruggedized case. As said, this is no notebook, just a portable PA-RISC workstations, implying that it does not have a battery but uses standard AC power input.

4.30.2 Internals

CPU

- PA-7100LC 60MHz with 1KB on-chip L1 and 64KB off-chip L1 cache
- PA-7100LC 80MHz with 1KB on-chip L1 and 256KB off-chip L1 cache

The 1KB on-chip L1 cache is not really a true cache.

Chipset

- LASI ASIC, which features:
  - NCR 53C710 8-bit single-ended SCSI-2
  - Intel 82596CA 10Mb Ethernet controller
  - WD 16C522 compatible parallel
  - Harmony CD/DAT quality 16-bit stereo audio
  - NS 16550A compatible serial
- Artist graphics, 8-bit
- Intel 82503 Ethernet transceiver, media auto-selection
- CS4215 or AD1849 programmable CODECs
- WD37C65C Floppy controller
- two AM29F010 Flash EPROMs

[154] http://www.saic.com

Display

- 10.4" active matrix LCD
- XGA resolution, i.e. 1024x768
- 256 colors (8-bit)
- 60Hz refresh

Human Input

- PS/2-compatible, 84-key integrated QWERTY-keyboard with 12 function keys
- Trackball and 3-button pad (left- or right-handed)

Buses

- GSC; system level I/O bus
- SCSI-2 Fast-Narrow single-ended bus

Memory

- Proprietary memory modules
- 32MB minimum, 128MB maximum

Expansion

- Two PCMCIA/PC card slots, supporting either two Type I/II or one Type III

Drives

- One 3.5" Fast-Narrow 50-pin SCSI-2 harddrive
- One 3.5", 1.44MB Floppy drive

4.30.3 External Connectors

- 50-pin HD SCSI-2 Fast-Narrow single-ended
- DB9 male RS232C serial (up to 115200 baud)
- DB25 female parallel
- TP/RJ45 10Mbit Ethernet
- 15-pin AUI 10Mbit Ethernet
- HD15 VGA
- two PS/2 connectors for keyboard & mouse
- three phone jacks (microphone, headphones and line-in)

4.30.4 Operating Systems

- HP-UX: every 32-bit release from 10.20 - 11.11 works.
  - 10.20: runs nice.
  - 11.00 and 11i: run ok.
- Linux: should work.
- NetBSD: should work.
- OpenBSD: works fine, although some I/O-devices are not supported at the moment (e.g. the PCMCIA-controller).

4.30.5 Benchmarks

Model	SPEC92, int	SPEC92, fp	SPEC95, int	SPEC95, fp
Galaxy 1100 80MHz	99	122	3.12	3.55

4.30.6 Physical dimensions

- 114*412*311 mm height*width*depth
- 8.2kg net weight

4.31 Stratus Continuum Servers

4.31.1 Overview

Stratus Technologies[155] builds a line of *Ultra High Availability Fault Tolerant* PA-RISC based servers called Continuum series. Several models were build over the years with an stated availability in the 99.999% range (and even higher). Thus, these systems feature a great deal of redundancy, peaking in having four CPUs to form one single logical processor. They are still actively sold.

4.31.2 Hardware Details

I/O

The Continuum 600 and 1200 series are basically the same system, except for the chassis configuration. The 600 has six slots for the main bus (called the Golf bus), and the rest of the space is filled with I/O card cages meant for secondary I/O boards. The 1200 has twelveslots for the main bus which occupies the entire width of the chassis. Secondary I/O boards go into a separate chassis. Both models have space for two rows of cooling fans on the top, and two rows of disk drives on the bottom (and also either a QIC or DAT tape drive or CDROM drive). The redundant power supplies with built-in UPS resides at the very bottom.

The main Golf bus is the main interconnect between the "big" boards. It is also redundant and self-checking. The "big" boards consist of the following (all these are FRUs):

- G7xx - CPU and memory boards (of different number and type of processors, speeds and memory sizes)
- K450 - 4-channel HVD fast wide SCSI and Ethernet adapter
- K460 - 4-channel HVD fast wide SCSI and Ethernet adapter
- K470 - A "carrier board" that can contain up to three PMC (PCI-mezzanine) daughter cards
- K600 - Adapter to two PK-buses which connects to the secondary I/O card cages

On the 600 chassis, the six slots consists of two for the pair or CPU/memory boards, and four more slots for two pairs of "big" boards. On the 1200 chassis, there are slots for two pairs of CPU/memory boards and four pairs of big boards.

In addition the 600/1200 main chassis also has a pair of Console Controller cards which provides the RS232 console terminal and RSN modem connectivity. This controller also has a command mode that allows the operator to type commands on the console to reset the system, power down, power up, etc. It runs on "housekeeping power" that is independent of the rest of the system. The Console controller also contains some environmental monitoring circuitry that checks the chassis internal temperature and will increase the cooling fan speed if necessary (the fans themselves are also hot-swappable FRUs).

The secondary I/O chassis can be used to plug in a wide array of I/O boards (all Stratus proprietary). These boards are also used on the XA/R line. FTX supported many of the communications boards

[155] http://www.stratus.com

(ISDN, serial, parallel, X.25, and all sorts of other comm boards). HP-UX did not support many of those, if any. VOS also supported disk and tape I/O through this.

Expansion chassis is available to house additional secondary I/O cards or disk shelves (for large disk farms, etc).

Architecture

Each logical processor is physically two pairs of actual CPUs (that means four physical CPU chips per single logical one).

Each pair is located on a separate FRU. All processors run "lock-stepped" (that is, they do exactly the same thing at the same time). Comparator logic between each two physical CPU pair monitors for discrepancies. If any physical CPU glitches or does something different, the comparator logic will detect the error and take that pair of CPUs offline, while the system continues to run on the other pair. There is no "failover time". On multi-processor boards, each FRU contains multiple pairs of the logical processor halves.

The memory is self-checking and ECC corrected. If an uncorrectable error occurs, the FRU in which the memory is located will also be taken offline.

The DMA engines for the big I/O boards is designed such that the main memory content is protected from an errant card from scribbling over addresses that it was not supposed to write to. This of course is programmed by the OS device drivers.

The big I/O boards are also self-checking and contain a pair of everything. However, with the exception of the K600 they do not run lock-stepped to the twin FRU. For example on the K450/K460 boards, each of the SCSI host adapters is connected via the backplane into the same SCSI bus on the partner board, but each board's controller occupies a different SCSI target ID. Only one controller is normally active, but when a failure occurs on the active board, all I/O is switched to the other controller. For the Ethernet ports on that board, they can be wired up to the same network or to different networks, and a software RNI (redundant network interface) layer provides transparent switching.

Other communications interfaces employ software-driven failover schemes.

All disks are mirrored. Early FTX 3.x releases used an in-house virtual disk layer (VDL) driver, but later releases switched to a modified version of the Veritas VxVM product. In HP-UX, HP's own LVM (logical volume manager) is used. VOS, of course, has its own disk mirroring scheme.

The Continuum 400 series has the same CPU/memory architecture as the 600/1200, but the I/O bus is different. Instead of a Golf bus, it has an "X" bus that connects each CPU/memory module to a pair of PCI bridge boards. All I/O connectivity is via PCI cards. There are two PCI bays of 7 slots each, connected downstream from the PCI bridge boards. Each bay has a dual channel SCSI adapter on it as standard equipment. These are also cross-wired and dual-initiated much in the same way as the SCSI ports on the 600/1200 systems. The 400 is also typically shipped with a pair of Ethernet adapter cards. The PCI bridge boards also each contains a removable PCMCIA flash memory card. This is used as the boot device. FTX puts the bootloader as well as the UNIX kernel on there, whereas HP-UX only uses it for the bootloader.

The PCI bay doors control the power the the PCI slots. Once opened, all slots in that bay are powered off to facilitate removal and insertion of cards. The system continues to run on cards in the

other bay. An interlock mechanism prevents both bay doors from being opened at the same time.

Again, all disks are mirrored as they are on the 600/1200 series, and communications interfaces use software-controlled failover mechanisms.

On the Continuum 400 the Console Controller is integrated into the CPU/memory FRUs. You can still reset the system via the "software front panel" on the console, but to power up/down you need to use the actual power switches on the machine (there are two, one for each power supply).

The Continuum 400 has two chassis versions, one is a short form-factor and AC powered only, and there is a tall CO (central office) version with a choice of AC or DC power. (*Thanks to Ti Kan for the input.*)

4.31.3 System Table

Model	CPU	Logical/ physical CPUs	Cache per CPU	max. RAM	Exp.	Storage	I/O	OS
419	PA-8500 360MHz	L1/P4	1.5MB	8GB	12 PCI	14 drives, 4 CD-ROMs, 4 tape-drives	16 10/100Mbit, 8 T1/E1, 64 Async, 64 RS232, 32 X.21, 32 V.35	HP-UX *(See Note 1)*, FTX *(See Note 2)*
429	PA-8500 360MHz	L2/P8	1.5MB	8GB	12 PCI	14 drives, 4 CD-ROMs, 4 tape-drives	16 10/100Mbit, 8 T1/E1, 64 Async, 64 RS232, 32 X.21, 32 V.35	HP-UX *(See Note 1)*, FTX *(See Note 2)*
439	PA-8600 480MHz	L1/P4	1.5MB	8GB	12 PCI	14 drives, 4 CD-ROMs, 4 tape-drives	16 10/100Mbit, 32 T1/E1, 64 Async, 64 RS232, 32 X.21, 32 V.35	HP-UX *(See Note 1)*, FTX *(See Note 2)*
449	PA-8600 480MHz	L2/P8	1.5MB	8GB	12 PCI	14 drives, 4 CD-ROMs, 4 tape-drives	16 10/100Mbit, 32 T1/E1, 64 Async, 64 RS232, 32 X.21, 32 V.35	HP-UX *(See Note 1)*, FTX *(See Note 2)*
610S	PA-7100 72MHz	L1/P4	512KB	128MB	6 slots			VOS, FTX *(See Note 2)*

610	PA-7100 72MHz	L1/P4	512KB	512MB	6 slots			VOS, FTX *(See Note 2)*
615S	PA-7100 96MHz	L1/P4	2MB	128MB	6 slots			VOS, FTX *(See Note 2)*
615	PA-7100 96MHz	L1/P4	2MB	1GB	6 slots			VOS, FTX *(See Note 2)*
616S	PA-8500 360MHz	L1/P4	1.5MB	0.5GB	6 slots			VOS, FTX *(See Note 2)*
616	PA-8500 360MHz	L1/P4	1.5MB	2GB	6 slots			VOS, FTX *(See Note 2)*
618	PA-8000 180MHz	L1/P4	2MB	3GB	6 slots			VOS, FTX *(See Note 2)*
619	PA-8500 380MHz	L1/P4	1.5MB	4GB	6 slots			VOS, FTX *(See Note 2)*
620	PA-7100 72MHz	L2/P8	512KB	512MB	6 slots			VOS, FTX *(See Note 2)*
625	PA-7100 96MHz	L2/P8	2MB	2GB	6 slots			VOS, FTX *(See Note 2)*
628	PA-8000 180MHz	L2/P8	2MB	3GB	6 slots			VOS, FTX *(See Note 2)*
629	PA-8500 380MHz	L2/P8	1.5MB	4GB	6 slots			VOS, FTX *(See Note 2)*
651-2	PA-8600 480MHz	L1/P4	1.5MB	4GB	6 slots			VOS, FTX *(See Note 2)*
652-2	PA-8600 480MHz	L2/P8	1.5MB	4GB	6 slots			VOS, FTX *(See Note 2)*
1210	PA-7100 72MHz	L1/P4	512KB	?	12 slots			VOS, FTX *(See Note 2)*
1215	PA-7100 96MHz	L1/P4	2MB	?	12 slots			VOS, FTX *(See Note 2)*
1218	PA-8000 180MHz	L1/P4	2MB	3GB	12 slots			VOS, FTX *(See Note 2)*

1219	PA-8500 380MHz	L1/P4	1.5MB	4GB	12 slots			VOS, FTX *(See Note 2)*
1220	PA-7100 72MHz	L2/P8	512KB	512MB	12 slots			VOS, FTX *(See Note 2)*
1225	PA-7100 96MHz	L2/P8	2MB	2GB	12 slots			VOS, FTX *(See Note 2)*
1228	PA-8000 180MHz	L2/P8	2MB	3GB	12 slots			VOS, FTX *(See Note 2)*
1229	PA-8500 380MHz	L2/P8	1.5MB	4GB	12 slots			VOS, FTX *(See Note 2)*
1245	PA-7100 96MHz	L4/P16	2MB	2GB	12 slots			VOS, FTX *(See Note 2)*
1251-2	PA-8600 480MHz	L1/P4	1.5MB	4GB	12 slots			VOS, FTX *(See Note 2)*
1252-2	PA-8600 480MHz	L2/P8	1.5MB	4GB	12 slots			VOS, FTX *(See Note 2)*

Notes

1. The HP-UX which runs on these systems is not a stock HP-UX, but a Stratus-modified HP-UX 11.00.

2. FTX, Stratus' own Unix System V Release 4 multiprocessor OS, is only offered on an exception basis. VOS runs from release 13.0 on PA-RISC hardware.

4.31.4 References

- **The Stratus Continuum Family**[156]
- **Stratus Continuum 400 Series**[157]
- **Stratus Continuum 600 and 1200 Series**[158]
- **Stratus Machine History**[159] by Paul Green

[156] http://www.stratus.com/products/continuum/
[157] http://www.stratus.com/products/continuum/s400/
[158] http://www.stratus.com/products/continuum/s600/
[159] ftp://ftp.stratus.com/pub/vos/doc/reference/machine_history.txt

4.32 HP 9000/520

(*Large parts contributed by Frank McConnell*)

4.32.1 Overview

Though the HP 9000/520 was not based on a PA-RISC CPU it is fair to say it was one of the predecessors of the PA-RISC workstations and the first member of the HP 9000 series.

The 9000/520 (originally 9020) was introduced in 1982 by HP and one year later described in the Hewlett Packard Journal as "[...] the new HP 9000 computer, a mainframe on the desktop [...]". All 500s used the same processors, memory and I/O; differences were in expandability and built-in I/O. The model 520 workstation was followed by the rack-mounted model 530 and the model 540 in a free-standing cabinet. HP 9000/500s in an SMP-configuration were confusingly also called *600 series*.

4.32.2 Hardware

The basic architecture of the 500 series was based on a processor architecture called FOCUS, compromising five NMOS-III ICs. It was a 32-bit segmented stack-architecture CPU, very similar to the original HP3000's 16-bit CISC CPU, bundled with an I/O processor (IOP), a memory controller. a 16Kx8 dynamic RAM and a clock driver. Due to heat dissipation difficulties the ICs were mounted on special printed-circuit boards called "finstrates" - the board has a 1mm copper sheet as core to which the IC substrate is epoxied directly.

The result of this were three finstrates: CPU, IOP and 256KB RAM, which were installed in a 12-slot module. This allowed configurations of up to 2.5 MBs of RAM; memory cards could be substituted to construct multiprocessor systems. The CPU, IOP and memory controller communicated via the memory processor bus (*MPB*). The protocol of this 44-line 36MB/s supports up to seven CPUs or IOPs and fifteen memory controllers. At least one IOP to interface with the I/O-buses was needed so up to six CPUs were supported in hardware.

A 9000/520 (*Dawn*) compromised the following hardware:

- CPU; each ran at a clock of 18MHz and executed up to 1M instructions per second
- IOP; each drove an proprietary I/O bus (CIO) that supported up to eight devices
- display, either color or monochrome
- keyboard
- floppy disk
- optional integrated thermal printer
- internal hard-disk

4.32.3 Architecture

The FOCUS is a stack architecture, with over 220 instructions (some 32 bits wide, some 16 bits wide), a segmented memory model, and no general purpose programmer-visible registers.

It has a flat address space but that is not really what most programs see. Programs' access to memory is largely described by registers that contain the absolute memory addresses of segment boundaries. For example, instructions come from the current code segment, which is described by three registers: `P`, the program counter, which is a 32-bit register containing the absolute address of the instruction being executed; `PB`, the program base register, which is a 32-bit register containing the absolute address of the first word of the current code segment; and `PL`, the program limit register, which is a 32-bit register containing the absolute address of the last word of the current code segment.

The data segment also has base (`DB`) and limit (`DL`) registers, and so does the stack segment (`SB`, `SL`). The stack segment also has a stack pointer (`S`) and a stack marker pointer (`Q`) which points to the current procedure's activation record on the stack.

There is also an index register, a status register, a flags register (really a sort of debugging-state register), a message register (interrupting conditions) and message mask register (which enables/disables interrupts from the message register), a breakpoint register, and a couple of registers which are for the memory controllers to talk to the CPU.

The machine instruction set is oriented toward moving words between memory and the top of the stack, and operating on the words at the top of the stack. So e.g. if you want to add two numbers you load one, load the other, execute an `ADD` instruction, and then a store instruction if you want to keep the result somewhere in memory other than on the stack.

The stack is in memory, there are probably some numbers of "top of stack" registers inside the processor to keep things moving relatively quickly, but these registers are not otherwise visible to the programmer.

4.32.4 Software

A choice of operating systems was provided by HP for the 520: HP BASIC or HP-UX. Both were built on top of a common kernel, called "SUN OS" (sic!) which provided basic operating primitives like memory, processor and I/O management. This was intended to be invisible to the user. HP-UX for the 9000/500 was in fact the first commercial UNIX supporting a multi-processor, multi-user system.

4.32.5 References

- A photo of a 9000/520. Gaby Chaudry
- An Usenet post from Roger N. Clark discussing the processing strenghts and benchmarks of the series 500. (from 1988)

4.33 PA-RISC Benchmarks

4.33.1 Overview

Some assorted benchmarks, compiled onto one page with available SPEC results for most PA-RISC systems. Other benchmarks (e.g STREAM) might be added later. Multi-CPU configurations are specially noted, otherwise the results are from single-CPU systems. Below this table is a table with results from other RISC-Workstations (and PCs) as a reference point to compare the data to.

For now there are results from three different benchmarks sets listed: SPEC92, SPEC95 and SPEC2000. Each set contains results for both integer- and FP-intensive CPU benchmarks, which emphasize the performance of the computer's CPU, memory-architecture and compiler. The SPEC95 *rate* column contains results for throughput-intensive integer and FP benchmarks, which measure the ability of a computer to carry out multiple tasks at the same time.

Model	SPEC92 int/fp	SPEC95 int/fp	SPECrate95 int/fp	SPEC2000 int/fp
705	21.9/33.0			
710	31.6/47.6	0.99/1.44		
712/60	67.0/85.3	2.08/2.66	18.7/23.9	
712/80	97.1/123.3	3.12/3.55	28.1/32.0	
712/100	117.2/144.2	3.76/4.06	33.8/36.3	
715/33	32.5/52.4	1.01/1.58		
715/50	49.2/78.8	1.53/2.46		
715/64	80.6/109.4	2.52/3.31		
715/75	82.6/127.2	2.51/3.85		
715/80	96.3/123.2	3.01/3.50		
715/100	115.1/138.7	3.76/4.03	30.0/38.3	
715/100XC	132.2/184.6	4.55/4.70	40.9/42.3	
720	36.4/58.2	1.20/2.00	14,1/18.2	
725/50		1.53/2.46		
725/75		2.51/3.85		
725/100		3.76/4.03		
730	47.8/75.4	1.50/2.30		
735/99		3.22/4.06	29.4/35.8	
735/125		3.97/4.61	36.3/40.9	
742i/50		1.53/2.46		
743i/64		2.52/3.31		
743i/100		3.76/4.03		
744/132L		6.45/6.70		
744/165L		7.90/7.64		
745i/50		1.53/2.46		
745i/100		3.22/4.06		
745/132L		6.45/6.70		
745/165L		7.90/7.64		
747i/50		1.53/2.46		
747i/100		3.22/4.06		
748i/64		2.52/3.31		
748i/100		3.76/4.03		
748/132L		6.45/6.70		
748/165L		7.90/7.64		

750	48.1/75.0	1.50/2.30		
755/99		3.22/4.06	29.4/35.8	
755/125		3.97/4.61	36.3/40.9	
A180/800				
A180C/800		9.22/8.60		
A400 *(rp2400)*				
A400-6X *(rp2430)*				
A500-44 *(rp2450)*				
A500-5X *(rp2450)*				422/414
A500-6X *(rp2470)*				
A500-7X *(rp2470)*				
B132L		6.45/6.70	58.1/60.3	
B132L+		6.84/7.17	61.5/64.6	
B160L		7.75/7.56	69.7/68.1	
B180L+		9.22/9.43	83.0/84.8	
B1000		23.90/39.30	217/378	
B2000		31.80/52.40	286/472	332/357
B2600				403/440
C100		4.98/6.59	44.8/59.4	
C110		6.00/8.14	54.0/73.3	
C132L		6.45/6.70	58.1/60.3	
C160L		7.75/7.56	69.7/68.1	
C160		10.40/16.30	93.6/147	
C180		11.80/18.70	107/169	
C200		14.20/21.40	129/193	
C240		17.10/25.40	156/229	
C360		26.00/28.10	234/252	
C3000		31.80/52.40	287/471	313/321
C3600		42.00/64.00	379/576	432/433
C3650				508/542
C3700				604/576
C3750				678/674
D200	115/146	2.18/2.90	19.2/25.8	
D210	152/194	3.74/4.08	33.6/36.7	
D220		6.57/6.72	59.2/60.5	
D230		7.87/7.58	70.8/68.3	
D250	144/218	5.01/6.77	45.1/61.0	
D250 2-CPU			89.0/106	
D260				
D260 2-CPU			114/143	
D270		10.40/15.0	93.9/135	
D270 2-CPU			184/190	
D280		12.30/17.40	111/157	
D280 2-CPU		12.30/17.40	219/221	
D300	115/146	2.18/2.90	19.2/25.8	
D310	152/194	3.74/4.08	33.6/36.7	
D320		6.57/6.72	59.2/60.5	
D330		7.87/7.58	70.8/68.3	
D350	144/218	5.01/6.77	45.1/61.0	

D350 2-CPU			89.0/106	
D360				
D260 2-CPU			114/143	
D370		10.40/15.0	93.9/135	
D370 2-CPU			184/190	
D380		12.30/17.40	111/157	
D380 2-CPU			219/221	
D390		15.50/25.50		
E25	45.0/66.7			
E35	65.6/98.5			
E45	82.1/122.9			
E55	108.0/163.4			
F10	22.0/36.6			
F20	33.6/56.1			
F30	37.8/62.4			
G30	37.8/62.4			
G40	65.2/91.3			
G50	100.0/158.5			
G60	108.8/195.3			
G70	108.8/195.3			
Galaxy 1100 80MHz *(SAIC)*		3.12/3.55		
H20	33.6/56.1			
H30	37.8/62.4			
H40	65.2/91.3			
H50	100.0/158.5			
H60	108.8/195.3			
H70	108.8/195.3			
I30	37.8/62.4			
I40	65.2/91.3			
I50	100.0/158.5			
I60	108.8/195.3			
I70	108.8/195.3			
J200		4.98/4.50	44.8/61.3	
J200 2-CPU			64.5/105	
J210		6.00/5.40	54.0/73.4	
J210 2-CPU			77.5/126	
J210XC		6.40/5.70	57.6/81.5	
J210XC 2-CPU			82.8/142	
J280		11.80/19.30	107/174	
J282				
J2240		17.40/26.30	157/237	
J2240 2-CPU			307/349	
J5000		32.50/54.00	302/486	
J5000 2-CPU			579/744	
J5600		42.60/62.70	384/564	408/392
J5600 2-CPU			758/847	
J6000		42.60/62.70	384/564	408/392
J6000 2-CPU			758/847	
J6700		57.60/85.90		469/581

J7000		32.50/54.00	302/486	
J7000 2-CPU			579/744	
K100		4.92/6.80		
K200		4.92/6.80	44.3/61.2	
K200 2-CPU			87.9/117	
K200 4-CPU			174/198	
K210		5.92/8.15	53.3/73.4	
K210 2-CPU			106/140	
K210 4-CPU			210/238	
K220		6.41/9.11	57.7/82.0	
K220 2-CPU			114/157	
K220 4-CPU			228/275	
K250		10.7/18.8	96.0/169	
K250 2-CPU			189/279	
K250 4-CPU			375/383	
K260		11.8/20.2	107/182	
K260 2-CPU			212/297	
K260 4-CPU			418/398	
K370		14.6/23.0	132/207	
K370 2-CPU			261/322	
K370 4-CPU			519/434	
K370 6-CPU			767/489	
K380		17.4/28.5	157/257	
K380 2-CPU			312/398	
K380 4-CPU			610/532	
K380 6-CPU			902/604	
K400		4.92/6.80	44.3/61.2	
K400 2-CPU			87.9/117	
K400 4-CPU			174/198	
K410		5.92/8.15	53.3/73.4	
K410 2-CPU			106/140	
K410 4-CPU			210/238	
K420		6.41/9.11	57.7/82.0	
K420 2-CPU			114/157	
K420 4-CPU			228/275	
K450		10.7/18.8	96.0/169	
K450 2-CPU			189/279	
K450 4-CPU			375/383	
K460		11.8/20.2	107/182	
K460 2-CPU			212/297	
K460 4-CPU			418/398	
K570		14.6/23.0	132/207	
K570 2-CPU			261/322	
K570 4-CPU			519/434	
K570 6-CPU			767/489	
K580		17.4/28.5	157/257	
K580 2-CPU			312/398	
K580 4-CPU			610/532	
K580 6-CPU			902/604	

L1000-36 *(rp5400)*				
L1000-44 *(rp5400)*				
L2000-36 *(rp5450)*				
L2000-44 *(rp5450)*		33.70/72.30		
PrecisionBook 132 *(RDI)*		6.49/6.54		
PrecisionBook 160 *(RDI)*		7.78/7.39		
PrecisionBook 180 *(RDI)*		9.22/9.43		
R380		12.30/17.40		
R390		15.50/25.50		
T500				
T520		5.24/?	47.2/	
T520 2-CPU			93.8/	
T520 4-CPU			186/	
T520 8-CPU			363/	
T520 12-CPU			531/	
T600		11.8/14.9	106/134	
T600 2-CPU			211/263	
T600 4-CPU			418/510	
T600 6-CPU			617/735	
T600 8-CPU			814/915	
T600 10-CPU			1003/1043	
T600 12-CPU			1192/1151	
V2200		13.8/22.1	125/	
V2200 4-CPU			484/755	
V2200 8-CPU			964/1380	
V2200 12-CPU			1442/1909	
V2200 16-CPU			1865/2312	
V2250				
V2250 16-CPU		16.4/24.8	2209/2471	
V2600				
V2600 16-CPU			5164/	
V2600 32-CPU			9315/	
SPP1000/CD *(Convex)*				
SPP1000/XA *(Convex)*				
SPP1200/CD *(Convex)*				
SPP1200/XA *(Convex)*				
SPP1600/CD *(Convex)* 8-CPU			290/383	
SPP1600/XA *(Convex)* 16-CPU			541/744	
SPP1600/XA *(Convex)* 32-CPU			996/1444	

4.33.2 Reference Results

Model	SPEC92 int/fp	SPEC95 int/fp	SPECrate95 int/fp	SPEC2000 int/fp
DEC 3000/500 A21064@150MHz	84.4/127.7	2.15/3.65		
DEC Alphastation 200 4/166 A21064@166MHz	107.7/134.8	2.31/3.22	20.8/29.0	

DEC PWS500au A21164@500MHz		15.7/19.5	142/175	161/158
IBM RS/6000 320H POWER@25MHz	20.9/39.4			
IBM RS/6000 43P MPC604@133MHz	176.4/156.5	4.72/3.76		
Sun SS5/110 MicroSP2@110MHz	78.6/65.3	1.59/1.99		
Sun Ultra2/2200 2xUltraSP@200MHz	332/505	7.88/14.7	145/188	
Sun Ultra10 UltraSP2i@440MHz			160/199	
Sun Ultra E450 4xUltraSP@296MHz		12.1/29.5	422/561	
AMD PC Athlon@650MHz		29.3/22.6		
Intel PC Pentium2@450MHz		17.6/13.1	158/118	
Intel PC Pentium3@1GHz		46.8/32.2		

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- **Model 715 Service Handbook** (http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37699/lpv37699.pdf) (PDF, 5.1MB)
- **Model 735 Service Handbook** (http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv38563/lpv38563.pdf) (PDF, 7.6MB)
- **Model 720/730 owner's guide** (http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37630/lpv37630.pdf) (PDF, 1.8MB)
- **743 Owner's Guide** (http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv38556/lpv38556.pdf) (PDF, 1.8MB)
- **743, 744 and 748 Technical Reference Manual** (http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00265/lpv00265.pdf) (PDF, 2.2MB)
- **Installing the A4505A PCI Module Upgrade** (http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00284/lpv00284.pdf) (PDF, 0.3MB)
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- **Installing Model 743 RAM Boards** (http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv00298/lpv00298.pdf) (PDF, 0.2MB)
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- **HP Pumps Up PA-8x00 Family** (http://web.archive.org/web/20040214112604/http://www.cpus.hp.com/technical_references/101996ar.shtml) (archive.org mirror) Description and results of the improvements made in PA-8200 and PA-8500. Linley Gwennap, October 1994, Microprocessor Report, Volume 10 Number 14.(Article reprint for vanished cpu.hp.com)
- **HP Pumps Up PA-8x00 Family** (http://web.archive.org/web/20040214112604/http://www.cpus.hp.com/technical_references/101996ar.shtml) (archive.org mirror) Description and results of the improvements made in PA-8200 and PA-8500. Linley Gwennap, October 1994, Microprocessor Report, Volume 10 Number 14. (Article reprint for vanished cpu.hp.com)
- **A 500 MHz 1.5 MByte Cache with On-Chip CPU** (http://ftp.parisc-linux.org/docs/whitepapers/isscc_cache_talk.pdf) (PDF, 141KB) Slides of a presentation on the PA-8500 CPU. Jonathan Lachman and J. Michael Hill, 1997, ISSCC.
- **PA-8500: The Continuing Evolution of the PA-8000 Family** (http://web.archive.org/web/20040214131135/http://www.cpus.hp.com/technical_references/8500.shtml) (archive.org mirror) Description of PA-8500 development and technical details. Gregg Lesartre and Doug Hunt, 1997, Proceedings of CompCon, IEEE CS Press. (Article reprint for vanished cpu.hp.com)
- **A 900MHz 2.25MByte Cache with On Chip CPU** (http://ftp.parisc-linux.org/docs/whitepapers/isscc_cache_talk_2.pdf) (PDF, 119KB) Slides of a presentation on the PA-8700 CPU, centered on the CPUs cache subsystem. J. Michael Hill and Jonathan Lachman, 2000, ISSCC.
- **HP Assembler Reference Manual** (http://docs.hp.com/hpux/onlinedocs/92432-90012/92432-90012.html) (HTML)
- **HP Assembler Reference Manual** (http://docs.hp.com/hpux/pdf/92432-90012.pdf) (PDF, 309KB)
- **Overview of the HP 9000 rp3410-2, rp3440-4, rp4410-4, and rp4440-8 Servers** (http://h71028.www7.hp.com/ERC/downloads/5982-4172EN.pdf) (PDF, 700KB) Technical Whitepaper from HP on new servers abd PA-8900 processor. Hewlett-Packard, 2005.

Chipsets

- **Hardball ERS** (http://ftp.parisc-linux.org/docs/chips/hardball_ers.pdf) (PDF, 4.2MB)
- **LASI ERS** (http://ftp.parisc-linux.org/docs/chips/lasi_ers.ps) (PS, 4.3MB)
- **Dino ERS** (http://ftp.parisc-linux.org/docs/chips/dino_ers.ps) (PS, 5.8MB)

- **Astro ERS Overview** (http://ftp.parisc-linux.org/docs/chips/astro_intro.ps) (PS, 0.1MB)
- **Astro ERS Error Handling** (http://ftp.parisc-linux.org/docs/chips/astro_errors.ps) (PS, 1.5MB)
- **Astro ERS R2I Operations** (http://ftp.parisc-linux.org/docs/chips/astro_ioc.ps) (PS, 2.3MB)
- **Astro ERS Register Map** (http://ftp.parisc-linux.org/docs/chips/astro_regmap.ps) (PS, 0.3MB)
- **Astro Runway Interface** (http://ftp.parisc-linux.org/docs/chips/astro_runway.ps) (PS, 2.0MB)
- **Astro Memory Map** (http://ftp.parisc-linux.org/docs/chips/astro_sysmap.ps) (PS, 0.1MB)
- **Elroy ERS** (http://ftp.parisc-linux.org/docs/chips/elroy_ers.ps) (PS, 4.7MB)
- **LSI 53C875E** (http://www.lsilogic.com/techlib/marketing_docs/storage_stand_prod/integrated_circuits/lsi53c875e_pb.pdf) (PDF, 0.3MB)
- **LSI 53C896** (http://www.lsilogic.com/techlib/marketing_docs/storage_stand_prod/integrated_circuits/lsi53c896_pb.pdf) (PDF, 0.2MB)
- **Design of the Model 712's I/O subsystem (LASI)** (http://www.hpl.hp.com/hpjournal/95apr/apr95a4.pdf) (PDF, HP Journal 4/95)
- **Runway Bus introduction** (http://www.hpl.hp.com/hpjournal/96feb/feb96a2.pdf) (PDF, HP Journal 2/96)
- **J/K-Class Memory System description** (http://www.hpl.hp.com/hpjournal/96feb/feb96a5.pdf) (PDF, HP Journal 2/96)
- **VISUALIZE Workstation Memory Subsystem** (http://h20000.www2.hp.com/bc/docs/support/SupportManual/lpv37826/lpv37826.pdf) (PDF, 120KB)

Miscellaneous Hardware

- **ADTX IDE-SCSI adapters** (http://mickey.lucifier.net/adtx/), as used in the RDI PrecisionBook
- **NetBSD 712 serial console HOWTO** (http://www.netbsd.org/Ports/hp700/serialconsole-712.html), instructions to configure your 712 to use serial console
- **Replacing the EEPROM on an HP J282** (http://www.lava.net/~kirill/j282/eeprom.html) (HTML). In case your J-Class needs a new EEPROM chip.

Other Resources

- **docs.hp.com - HP Technical Documentation archive.** (http://docs.hp.com/)
- **docs.hp.com - development tools and distributed computing** (http://docs.hp.com/hpux/dev/index.html) (HTML)
- **HP firmware upgrades for PA-RISC systems** (ftp://ftp.itrc.hp.com/firmware_patches/hp/cpu/) (FTP)