PRODUCT OVERVIEW
NOVEMBER 2002

CRAY X1
EXTREME PERFORMANCE

CRAY DESIGNED/BUILT/SERVICED

CRAY SOLUTIONS

EN ROUTE TO SUSTAINED PETAFLOPS COMPUTING

The Cray X1™ product is a major milestone en route to Cray's goal of delivering, by 2010, the world's first supercomputer able to sustain petaflops speeds (10^{15} calculations/second) on a variety of challenging applications. Problems identified as needing this extreme performance include drug discovery, energy and transportation investment modeling, nanotechnology, severe storm forecasting and climate modeling, planning for natural pandemics and bioterrorism, and more.

HIGH-EFFICIENCY / EXTREME PERFORMANCE

The Cray X1 system, designed to be the world's most powerful supercomputer product, features ultra-fast (12.8 gigaflops) individual processors, up to 819 gigaflops of peak computing power in a single chassis, and a high-bandwidth, low-latency interconnect for substantially more efficient scaling than on clustered SMP systems. The Cray X1 system is available with up to 52.4 teraflops of peak computing power.

The Cray X1 supercomputer is the successor to Cray MPP and vector products. Programmers with experience using clustered systems will also find the Cray X1 environment familiar: MPI, cache-based, distributed shared memory, 32- and 64-bit IEEE support. Co-array Fortran and UPC are available for leading-edge work benefiting from very low latency.

This high-efficiency, extreme-performance system is aimed at the critical computational needs of classified and unclassified government research, weather and environmental, automotive and aerospace, chemical and pharmaceutical, and academic research.

SCALABLE SYSTEM ARCHITECTURE

The Cray X1 system architecture is highly innovative, and is the first system of any kind designed from the processor up for efficient scalability. Full support for scalability is built directly into the processor itself, enabling a more efficient, tightly-coupled MPP architecture. Components contributing to scalability include:

DISTRIBUTED SHARED MEMORY (DSM)

The Cray X1 supercomputer is the first system to combine vector processing with a DSM system architecture. This architecture is characterized by memory that is physically distributed with each processor, yet logically shared by all processors in the system. This allows direct load/store access to all memory in the system.

SCALABLE CACHE COHERENCE PROTOCOL

The coherence protocol can efficiently handle the explicit communication found in distributed memory applications, without the overhead associated with SMP coherence protocols.

SCALABLE ADDRESS TRANSLATION

The address translation mechanism performs virtual-to-physical address translation at the remote node, requiring each node to keep track only of the translation information for local memory, not the entire machine. This provides the ability to scale to very large configurations without worrying about TLB faults.

INNOVATIVE NEW INSTRUCTION SET ARCHITECTURE (ISA)

Cray has put 30 years of experience and 10 years of active research into the design of a new instruction set for the Cray X1 system. This new ISA is expected to support at least a decade of new developments in technology.

The new ISA is an important step forward in high-performance processor design. The modernized ISA was designed with simplicity in mind – using simple instructions, while eliminating overly complicated and redundant instructions. The ISA includes a very large register file, support for 32-bit and 64-bit computation, new synchronization features for scalability, and more.

The Cray X1 system's vector ISA has several advantages – very high computational parallelism with minimal instruction throughput, low control complexity and power consumption per operation, excellent memory latency tolerance. These advantages combine to alleviate instruction bottlenecks.

ADVANCED CRAY X1 OPERATING SYSTEM

The operating system for the Cray X1 supercomputer, UNICOS/mp, is a scalable distributed-execution software system that is targeted to scale to a maximum single system image (SSI) of 1024 node modules (4096 MSPs) and can be administered from a single point of operation.

The extended UNIX functions optimized for UNICOS/mp include:

UNICOS/mp runs across all node modules on a Cray X1 system. The distribution architecture within UNICOS/mp drives both system and applications node modules to run user commands and application commands, respectively.

UNICOS/mp provides kernel services and I/O to direct-attached disks; it also interfaces to the Cray Programming Environment Server (CPES) via a FibreChannel network interface.

UNICOS/mp supports accelerated application execution for distributed memory applications that use MPI, UPC or Fortran CoArrays. This acceleration is supported by special Cray X1 system memory mapping hardware to guarantee peak application performance in tightly synchronized environments.

UNICOS/mp supports both interactive and batch processing, executing simultaneously if desired.

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TECHNICAL DATA

CRAY X1
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CRAY X1 SYSTEM CONFIGURATIONS

CABINETS	CPUs	MEMORY	PEAK PERFORMANCE
1*	16	64 - 256 GB	204.8 Gflops
1	64	256 – 1024 GB	819 Gflops
4	256	1024 – 4096 GB	3.27 Tflops
8	512	2048 – 8192 GB	6.55 Tflops
16	1024	4096 – 16384 GB	13.1 Tflops
32	2048	8192 – 32768 GB	26.2 Tflops
64	4096	16384 – 65536 GB	52.4 Tflops

TECHNICAL SPECIFICATIONS

PEAK PERFORMANCE	52.4 Tflops in a 64 cabinet configuration
ARCHITECTURE	Scalable Vector MPP with SMP nodes

PROCESSING ELEMENT

PROCESSOR	Cray custom design vector CPU
	16 vector floating-point operations/clock cycle
	32- and 64-bit IEEE arithmetic
LOCAL MEMORY	16 to 64 GB per system module
DATA ERROR PROTECTION	SECDED
VECTOR CLOCK SPEED	800 Mhz
PEAK PERFORMANCE	12.8 Gflops per CPU
PEAK MEMORY BANDWIDTH	34.1 GB/sec per CPU
PEAK CACHE BANDWIDTH	76.8 GB/sec per CPU
PACKAGING	4 CPUs per node
	Up to 4 nodes per AC cabinet
	Up to 16 nodes per LC cabinet

MEMORY

TECHNOLOGY	RDRAM with 204 GB/sec bandwidth per node
ARCHITECTURE	Cache coherent, physically distributed, globally addressable
TOTAL SYSTEM MEMORY	32 GB to 64 TB

INTERCONNECT NETWORK

TOPOLOGY	Modified 2D torus
PEAK GLOBAL BANDWIDTH	400 GB/sec for a 64-CPU Liquid Cooled (LC) system

I/O

I/O SYSTEM PORT CHANNELS	4 per node module
PEAK I/O BANDWIDTH	1.2 GB/sec per SPC channel

PHYSICAL CHARACTERISTICS

AC MAINFRAME FOOTPRINT	35.5 in x 59.75 in per mainframe cabinet or .9 m x 1.5 m per mainframe cabinet
LC MAINFRAME FOOTPRINT	50.75 in x 103 in per mainframe cabinet or 1.3 m x 2.6 m per mainframe cabinet
I/O CABINET FOOTPRINT	29.5 in x 42.75 in per I/O cabinet or .75 x 1.1 m per I/O cabinet
AC MAINFRAME WEIGHT	~1973 lbs. or 895 Kg maximum per mainframe cabinet
LC MAINFRAME WEIGHT	~5754 lbs. or 2610 Kg maximum per mainframe cabinet
I/O CABINET WEIGHT	~1128 lbs. or 512 Kg maximum per I/O cabinet

*Note: Configuration available in Air Cooled (AC) model only

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